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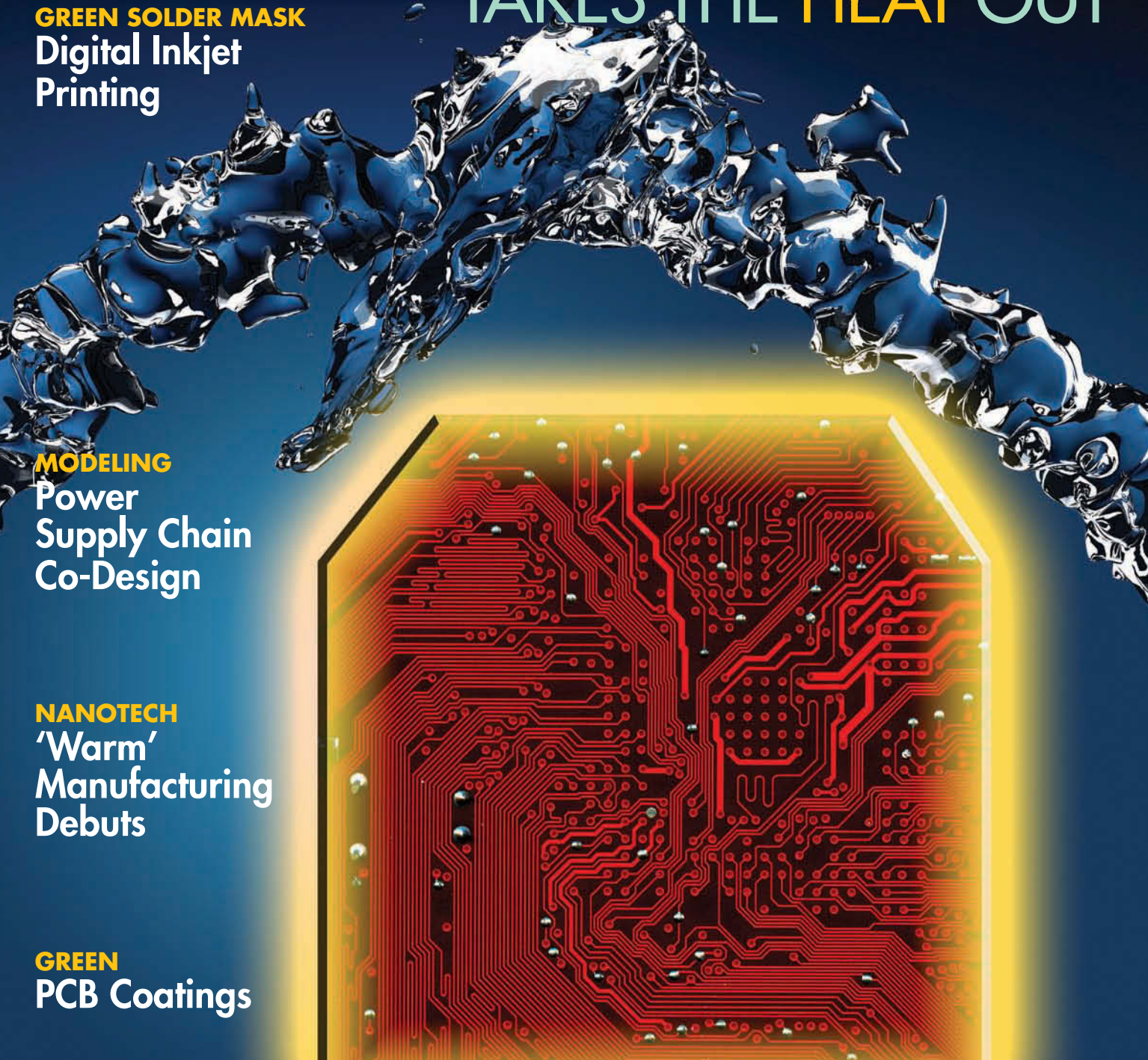
**GREEN SOLDER MASK**  
Digital Inkjet  
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**MODELING**  
Power  
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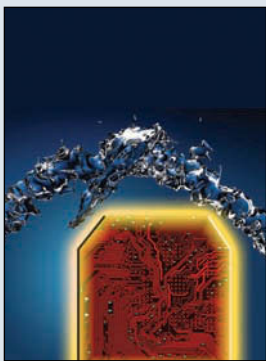
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Thermal issues effect electronic equipment performance. Thermal modeling, innovative materials and the use of a systems design approach can take the heat out.

Images © iStockPhoto.com/Evgeny Kuklev (water); Jakub Semeniuk (circuits). Design by Katherine Haddox

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### 'Web Circuits'

A major OEM has five boards with OSP finish requiring four additional components and the boards. Most companies would re-spin the design. But there's a less expensive, more elegant solution. **by MIKE BUETOW**

### A Novel Non-VOC Conformal Coating

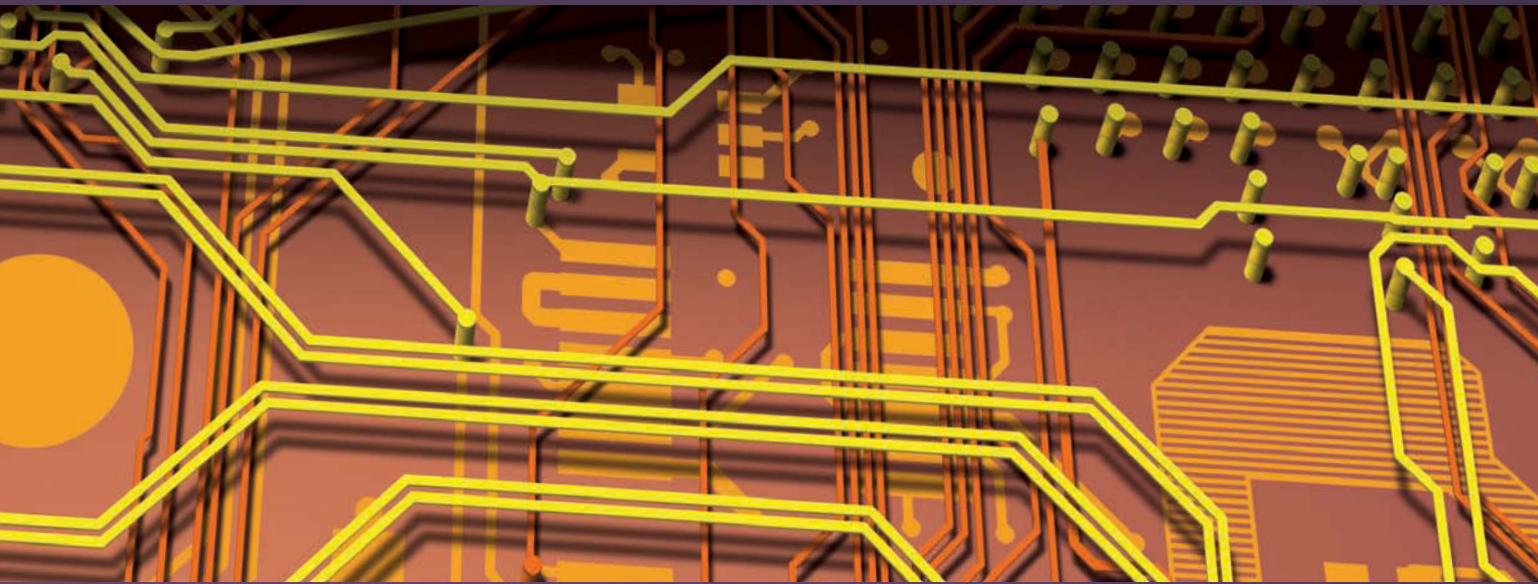
Moisture-cure coatings tend to be fast-reacting and could block machines. New chemistries, however, have led to a polyurethane pre-polymer, 100% solids material that performs well in SIR and thermal shock tests. **by JADE BRIDGES**



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KATHY  
NARGI-TOOTH

# What Keeps You Up at Night?

A few years ago, when I was working for a chemical supplier, I chaired the PCB Suppliers Leadership Meeting Subcommittee, part of the IPC Suppliers Council. As a matter of course we held annual meetings and inevitably the final afternoon session would turn into a roundtable discussion where we could vent on the latest series of challenges facing the industry. I don't think we solved many problems in those two-hour therapy sessions, but they were extremely cathartic, so we continued to include them in the program.

Over the past few years, the need for this type of open dialog between companies and within our industry has grown exponentially. We face very serious challenges today and will continue to be stress-tested in the years to come. While peer discussions may not help us solve all the problems, this constructive interaction and the precipitating brainstorm that results can certainly help us focus on those things most critical for success.

One of the biggest hurdles to address, especially in technology sectors, is our aging workforce. Don't get me wrong – I'm rapidly becoming one of them – but it has been estimated that nearly 50% of U.S. scientists and engineers will reach retirement age by 2012. They may not all retire then, but as they exit the workforce there are limited resources waiting in the wings. By 2013 the number of workers 54 to 64 years of age in the U.S. will mushroom to 12 million. Meanwhile, the younger, yet still experienced, workers – those aged 35 to 44 – will shrink by 15%. As a result there will be a labor shortage of major proportion, particular for highly skilled positions.

We know from analysis of our annual Salary Survey that the average age of the PCB designer rises each year. There are not enough engineers entering the field to offset the advancing age of the bulk of U.S. PCB designers. In 2007, the average age for PCB designers responding to our survey was 48, up from 46.8 in 2006. In all likelihood, the age will advance to over 49 in the 2008 survey. This should be a call to action for our industry. From where are the new engineers that will be needed over the next five to 10 years going to come?

We can all appreciate the relentless progression of technology, Moore's Law marching to its own drummer. But have you considered that such rapid advancement in technology is creating enormous education gaps? The half-life of an engineer's knowledge is considered to be five years. In the electronics industry it's even worse. More than 50% of what you learn as a freshman is obsolete by the time you reach your senior year. The only answer to keeping up and moving ahead is to actively engage in continuous training and re-education.

Today, 80% of the jobs available in the U.S. require some postsecondary educational schooling. While 97% of high school students hope to go to college, only 63% enroll, and of those, just 30% actually receive a bachelor's degree. It is estimated that the shortage of skilled workers in the U.S. will be over 5 million in 2010 and will swell to 14 million in 2015. This is the making of a real infrastructure disruptor.

So, ensuring the education and technical competence of young people entering the workforce is at the top of my list of things that keep me up at night. UP Media Group continues to support such educational activities. Through a variety of venues like the PCB Shows conferences, Webinars, the Virtual PCB event, in the magazine and on the web pages for *PCD&F*, there are daily opportunities to keep up to date. Make sure you check out the program for this year's PCB West included in this issue. The conference will be held Sept. 14 – 19 in Santa Clara, CA. I look forward to seeing you all there.

We are only as good as our information is timely and we want to ensure we are supplying more of the type of information and educational materials you need. Over the next few months we will be contacting you to get your opinion on the critical topics for the next 18 to 24 months. Make a point to participate in these surveys. Further, during PCB West, we will host a special event: Designer Decision 2008. This new feature offers an opportunity to share pressing concerns, technology-related issues or other industry problems. The results of our survey and forums will form the foundation of editorial coverage for *PCD&F* in 2009, so we hope that you will share with us what keeps *you* up at night.

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## SEMIS ASCEND

## Trends in the U.S. electronics equipment market (shipments only).

	FEB.	% CHANGE MAR. <sup>†</sup>	APR. <sup>*</sup>	YTD
Computers/electronics products	-8.8	-0.8	5.1	1.3
Computers	-1.7	-4.2	-13.6	-3.7
Storage devices	-0.1	1.7	-0.6	12.1
Other peripheral equipment	-2.0	2.7	7.0	4.6
Nondefense communications equipment	-1.4	1.1	-4.2	-2.1
Defense communications equipment	12.6	4.4	-6.7	27.1
A/V equipment	-7.0	-1.2	17.4	-12.0
Semiconductors	-31.2	-5.5	35.4	-4.5
Components <sup>1</sup>	-2.9	1.0	1.6	0.0
Nondefense search and navigation equipment	-17.5	0.8	-1.7	3.9
Defense search and navigation equipment	-4.1	2.2	-4.2	0.7
Medical, measurement and control	-5.4	-1.6	8.5	10.5

<sup>†</sup>Revised. <sup>\*</sup>Preliminary. <sup>1</sup>Includes semiconductors. Seasonally adjusted.  
Source: U.S. Department of Commerce Census Bureau, June 3, 2008

## Manufacturing Stalls Again in May

**TEMPE, AZ** – Economic activity in the manufacturing sector again failed to grow in May, as the PMI was 49.6%, up one point from April, says the Institute for Supply Management (ism.ws).

New orders were 49.7%, up 3.2 points sequentially, while inventories remained at 48%. Customer inventories were 47%, up two points, and backlogs were down 5.5 points sequentially, to 46%. Production bounded 2.1 points higher, to 51.2%, however.

A monthly PMI above 50% indicates that the manufacturing economy is generally expanding. A PMI over 41.1%, over a period of time, generally indicates an expansion of the overall economy. The average PMI year-to-date (49.2%) corresponds to a 2.5% increase in real GDP.

	JAN.	FEB.	MAR.	APR.	MAY
PMI	50.7	48.3	48.6	48.6	49.6
New orders	49.5	49.1	46.5	46.5	49.7
Production	55.2	50.7	48.7	49.1	51.2
Inventories	49.1	45.4	44.9	48.1	48.0
Customer inventories	49.5	49.0	51.0	45.0	47.0
Backlogs	44.0	45.0	47.5	51.5	46.0

Source: Institute for Supply Management, June 2, 2008

## METALS PRICES

	6/11/07	3/10/08	4/7/2008	5/6/08	6/2/08
Gold <sup>1</sup>	650.30	969.25	929.00	880.00	888.25
Silver <sup>2</sup>	188.29	294.94	266.27	248.71	246.52
Copper <sup>3</sup>	2.80	3.93	3.96	3.93	3.62
Tin <sup>4</sup>	6.28	8.73	9.28	10.99	9.60

<sup>1</sup>2nd London Fix - COMEX Gold. <sup>2</sup>Handy and Harman Silver (COMEX Silver). <sup>3</sup>LME Cash Seller and Settlement for Copper. <sup>4</sup>LME Cash Seller and Settlement for Tin

## EMS Set to Undergo Slowdown

**EL SEGUNDO, CA** – iSuppli Corp. (isuppli.com) in May trimmed its long-term forecast for global EMS revenue to 8% during the 2006 to 2013 timeframe, down from its previous outlook of 9.3% growth.

The research firm cited the combined size of the EMS and ODM businesses – \$305 billion – which hampers growth rates. Adam Pick, principal analyst for EMS/ODM, also pointed to a deceleration at Foxconn (fih-foxconn.com), the largest player. Finally, many EMS/ODM companies are rethinking their strategy of market share expansion in favor of competitive positioning and financial performance.

## Display Driver Chip Market Heads to Mature Stage

**EL SEGUNDO, CA** – Unit shipment growth for display drivers will slow to 15.1% in 2008, down from 26.2% in 2007, iSuppli Corp (isuppli.com) said. Annual growth will average about 11% from 2009 to 2011.

iSuppli estimates 6.9 billion units were shipped in 2007, up from 5.5 billion units in 2006, driven by LCD TVs and notebook PCs. Another factor: active matrix TFT-LCD displays found in many mobile and handheld products. Global revenue failed to keep pace, rising 10.2% to reach \$8.8 billion.

New applications and products like DPFs, multi-touch panels and 3-D displays should help expand the display market, iSuppli believes.

## WSTS Global Semi Growth 4.7% in 2008, 5.8% in 2009

**SEATTLE** – The global semiconductor market is expected to grow 4.7% to \$267.7 billion this year, up from 3.2% in 2007, according to the revised forecast of the World Semiconductor Trade Statistics (wsts.org). The WSTS lowered its projections by 4.4 points from its last forecast in November, mainly as a result of a weak fourth quarter 2007.

Demand is improving, however, leading the group to reiterate 2009 and 2010 projections of 5.8% and 8.8% growth, respectively.

## INDUSTRY MARKET SNAPSHOT

## Book-to-bills of various components/equipment.

	DEC.	JAN.	FEB.	MAR.	APR.
Semiconductor equipment <sup>1</sup>	0.85	0.89	0.92	0.87 <sup>†</sup>	0.81 <sup>P</sup>
Semiconductors <sup>2</sup>	3.27%	1.70%	1.35%	1.82% <sup>†</sup>	3.82% <sup>P</sup>
Rigid PCBs <sup>3</sup> (North America)	1.01	0.97	0.99	1.00	1.01
Flexible PCBs <sup>3</sup> (North America)	1.00	0.96	0.96	0.99	0.99
Computers/electronic products <sup>4</sup>	4.94	4.77	4.99	5.18 <sup>†</sup>	5.23 <sup>P</sup>

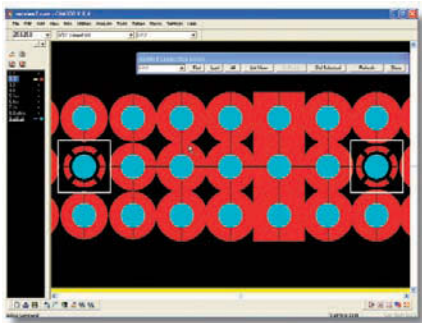
Sources: <sup>1</sup>SEMI, <sup>2</sup>SIA (3-month moving average growth), <sup>3</sup>IPC, <sup>4</sup>Census Bureau, <sup>P</sup>Preliminary, <sup>†</sup>Revised

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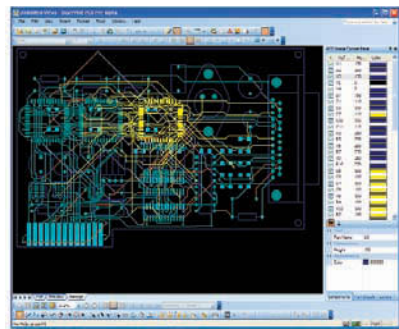
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## BROMINE'S GREEN LIGHT

## CASH CRUNCH

## Ban Lifted on Deca-BDE Flame Retardants

**STOCKHOLM, SWEDEN** – With legal action pending by the EU, the Swedish government lifted its national ban of the flame retardant Deca-BDE used in textiles, furniture and some electronic cables. The Swedish government said that the ban was inconsistent with the latest findings of a 10-year EU risk assessment of Deca-BDE. The 10-year risk assessment failed to identify any significant risks to justify restrictions on the flame retardant. The limited ban that went into effect in late 2006 reportedly had no scientific basis, and was therefore subject to a legal challenge by EU authorities.

“The EU has established that Deca-BDE is safe for continued use in all its applications, so there is no scientific basis whatsoever for any national or EU-wide restriction on Deca-BDE” said Veronique Steukers, chair of the European Brominated Flame Retardant Industry Panel (EBFRIP). The “EBFRIP firmly believes that Deca-BDE meets the criteria for an exemption from RoHS and that it should therefore either be exempted or deleted from the RoHS Directive. We are working with the European Commission to ensure that this restriction is lifted.”

The Swedish Government's press release can be found at: <http://www.regeringen.se/sb/d/10626/a/104665>.

## Chemical Suppliers Increasing Prices

**THE US AND EUROPE** – The Huntsman Corp., Dow Chemical, Dupont and Rohm & Haas have all announced plans to increase prices or add surcharges, as much as 25%, because of increasing energy and raw-material costs.

Huntsman joins the current trend in the chemical industry to pass on higher costs for energy and petroleum-based chemical ingredients to customers. Dow Chemical Co., the biggest U.S. chemical maker, said it would raise its prices as much as 20%, reportedly the highest in company history.

Dow claims its costs for raw materials to make plastics, and cost for the natural gas that powers its factories has jumped 42% in the first quarter from the same period in 2007. These expenses may continue to rise into the current quarter, according to a report quoting Dow CEO Andrew Liveris.

DuPont has also boosting prices, while Rohm & Haas Co has implemented surcharges on all products to recoup rising raw-material costs.

In Europe, Ciba Holding AG, Lanxess AG and Clariant AG are among the chemical producers also increasing prices in response to rising costs.

“We hope we have seen the worst of the energy and commodity price increases,” Huntsman CEO Peter Huntsman said in a statement. “The impact of large-scale speculation by traders on the price of energy, in addition to the increased costs we are absorbing from our raw-material suppliers and service providers, cannot be underestimated.”

## Global PCB Market Continues to Grow

**FRANKFURT, GERMANY** – According to the ZVEI, the worldwide PCB market grew by 8.7% in 2007 (as compared to the previous year) to \$51.5 billion. The organization states that for 2008, a global growth of over 8% is predicted.

According to the organization, the largest revenue share in 2007, at about 73%, was reported for Japan and Southeast Asia (including China). Japan accounted for \$9.5 billion (up 3.8%) and Southeast Asia for \$28.1 billion of revenue. The largest increase was reported for Southeast Asia, which at \$2.7 billion, was an increase of 10.6%. The report states that the American market grew by 3.3% to \$6.3 billion.

Also, according to the report, 2007 was the first year that Europe outpaced America. The market volume in Europe rose

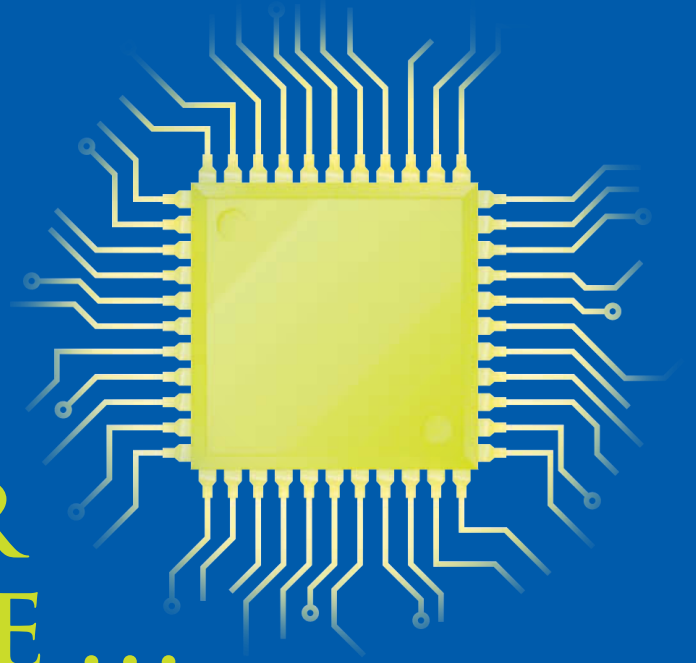
14.3% to \$6.4 billion, as compared to the U.S.'s previously stated \$6.3 billion.

The organization cited the high price levels for raw materials in 2007, and its affect on the industry, claiming that copper and crude oil prices were of greatest concern in countries such as China and India, given their high demand for raw materials, and that the rise in crude oil prices also raised the costs of paints, epoxy resins, films and resists.

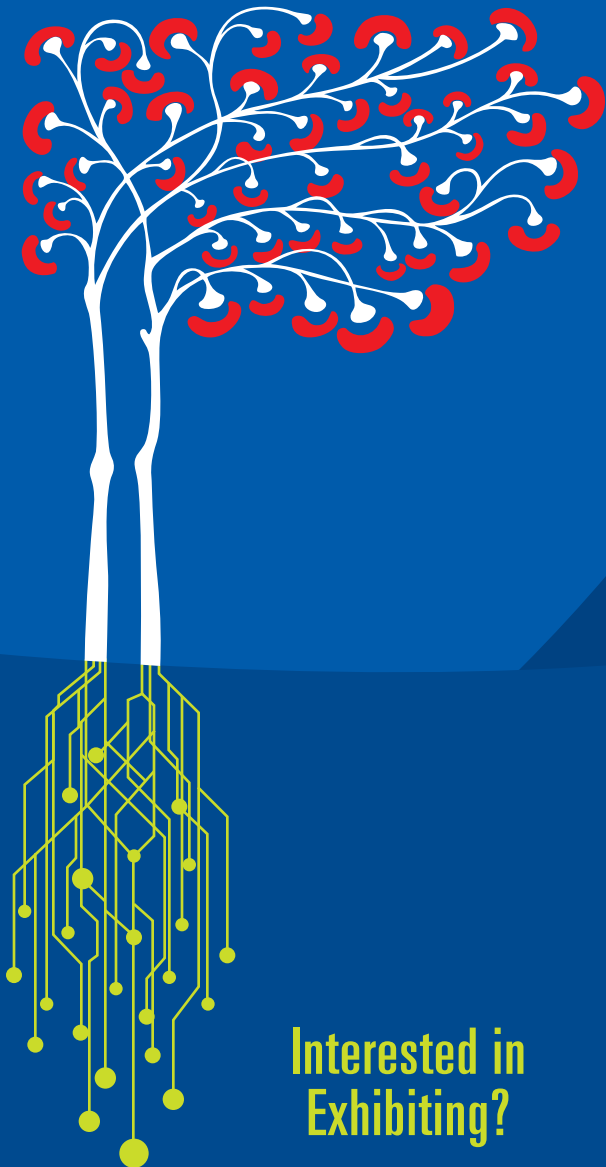
The ZVEI report states that while production volume in Europe in 2007 declined 8% year-over-year to 2.5 billion (\$3.86 million) and the number of registered manufacturers declined by 7%, the European PCB industry as a whole employed about 24,000 at the end of 2007, which is unchanged from 2006.



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## in BRIEF

**Valor Guiding Chinese Design Education.**

**SHENZHEN, CHINA** – Valor computerized Systems has signed an agreement establishing a technological partnership with the Guilin University of Electronic Technology (GUET). Valor and GUET will cooperate to encourage technical talent and develop and promote new technology within the industry. Valor provided GUET with software, including DFM, SMT programming, optimization, program conversion and process engineering, to be integrated into courses in undergraduate and postgraduate studies programs.

**Eastern European Expansion.** **ORADEA, ROMANIA** – Connectronics Romania has opened a 16,000 square meter factory with capacity for more than 1,000 employees. The factory in Romania will produce printed circuit boards and wiring harnesses for the automotive and telecommunications sectors. The Connect Systems group currently has eight factories in Europe.

**Fair Trade.** **SAN JOSE, CA** – The Semiconductor Industry Association (SIA) has announced its strong support for the Office of the United States Trade Representative (USTR) in its efforts to protect tariff-free trade in electronic products. These products have been duty-free since the implementation of the Information Technology Agreement (ITA) in 1997. “Free and fair trade is vitally important to the health of the U.S. semiconductor industry,” said SIA president George Scalise.

**Nanotech Health Risks.** **NEW YORK** – Increasing concern over emerging scientific evidence that nanoparticles may cause adverse health risks could put pressure on officials to produce regulations governing the use of nanotechnology. A study published this month in *Nature Nanotechnology* found that at least one nanomaterial, carbon nanotubes, appears to mimic the behavior of cancer-causing asbestos in the lung.

## Waste Not, Want Not

## Scrap PCBs Turned into “Liquid Gold”

**ROMANIA AND TURKEY** – Scientists claim to have found a method to turn PCBs into material suitable as fuel, or for industrial use.

In a recently released report called *Feedstock Recycling from the Printed Circuit Boards of Used Computers*, the process reportedly reduces the remains of a printed circuit board to a material called pyrolysis oil, which can be further refined like petroleum for fuel, or can be used by industries to make other chemicals.

While the researchers noted that the waste equipment was difficult to recycle because of additives, heavy metals, and toxic flame retardants contained in PCBs, in their report, the scientists describe the steps used to eliminate or remove almost all of the hazardous compounds from the material.

The process reportedly uses high temperatures, catalysts, and chemical filtration to remove the toxic elements, with the end result being an oil that can be safely used as fuel or raw materials for a number of consumer products.

## Cadence and Mentor Graphics Publish Book on OVM

**SAN JOSE, CA AND WILSONVILLE, OR** – Cadence Design Systems and Mentor Graphics have announced the publication of a book on Open Verification Methodology (OVM). The *Step-by-Step Functional Verification with SystemVerilog and OVM* is written by Dr. Sasan Iman.

The book provides a claimed guide and reference for adopting a functional verification methodology, learning the SystemVerilog language, and using the OVM library to build a verification environment for a realistic design example. The book reportedly contains more than 500 pages of original technical content.

“Dr. Iman brings together all the essential elements to understand the use and application of the OVM,” said Dennis Brophy, director at Mentor Graphics. “This book has everything design and verification engineers would want to know to apply the OVM to their most pressing challenges.”

“This book walks the reader through the OVM as well as the SystemVerilog language constructs upon which it is built. The breadth of this book and its pragmatic approach make it an invaluable resource for both novice and experienced verification engineers,” said Ted Vucurevich, CTO at Cadence.

## Latest OEM Push to “Green” Needs More Science

**USA, ASIA** – PC and electronics vendors including Dell, HP, Samsung and Sony have requested that copper clad laminate (CCL) manufacturers begin incorporating lead- and halogen-free materials into component production. The companies have also have asked that CCLs be completely free of these materials by late 2009, according to industry reports.

The primary halogen found in laminate materials is bromine and the source is typically TBBPA. In an exhaustive human health and environmental risk assessment conducted in the EU, where TBBPA was found to be safe for as a monomer to be reached with epoxy resins for the manufacture of printed circuit board laminate materials.

Currently, the level of lead- and halogen-free CCLs used in the industry is only 3% to 5%, but electronics makers moving

toward “green” technologies are expected to push the rate to 30% within the next 18 months, reports say. The rationale for this move is not based on the current science.

Industry sources report that only Iteq, Hitachi, Nanya PCB and Panasonic are currently producing halogen-free CCLs, and that costs for the use of traditional materials such as FR-4 are rising, but some companies say that production for traditional CCL products will not likely decline soon due to demand from China-based customers.

In one study related to the cost of implementing halogen free laminates, it was determined the transition could more than double the cost of traditional TBBPA based FR-4 materials. In an industry still reeling from the massive cost increases that accompanied RoHS regulation compliance, putting more bad science ahead of real science, begs the question, “Where the benefit?”

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## EVENTS

<b>15-17 Componex Nepcon Chennai 2008</b> Chennai Trade Center Chennai, India Contact: componex-nepcon.com  <b>15-17 Semicon West</b> Moscone Center San Francisco, CA Contact: semiconwest.org/index.htm  <b>28 2009 iNEMI Roadmap Workshop – Asia</b> Shanghai, China Contact: inemi.org	JULY	
<b>17-21 SMTAI 2008</b> Disney's Coronado Springs Resort Lake Buena Vista, FL Contact: smta.org; joann@smta.org  <b>18-22 IEEE EMC 2008</b> Cobo Center Detroit, MI Contact: scott@emcsociety.org	AUGUST	
<b>2-5 ElectronicIndia 2008</b> Bangalore, India Contact: global-electronics.net/link/en/16545148  <b>7-12 30th Annual EOS/ESD Symposium</b> Westin La Paloma Resort Tucson, AZ Contact: esda.org/symposia.html  <b>14-19 PCB WEST 2008</b> <b>MARRIOTT SANTA CLARA</b> <b>SANTA CLARA, CA</b> <b>CONTACT: FRANCES STEWART, FSTEWART@</b> <b>UPMEDIAGROUP.COM; KAMDEN ROBB, KROBB@</b> <b>UPMEDIAGROUP.COM; PCBWEST.COM</b>  <b>20-25 IPC Midwest Conference &amp; Exhibition</b> Renaissance Schaumburg Hotel & Convention Center Schaumburg, IL Contact: Maria Labriola, marialabriola@ipc.org	SEPTEMBER	
<b>21-23 Mexitronica</b> Guadalajara, Mexico Contact: www.mexitronica.com  <b>22-24 TPCA Show</b> Hosted by TPCA Taipei, Taiwan Contact: http://www.tpca.org.tw	OCTOBER	

**Zuken** has announced a partnership to provide schematic capture and PCB design to **MBDA European Missile Systems**, which produces programs for missile systems and countermeasures and manages multi-national defense projects in the EU. Zuken's schematic and PCB design software was selected to standardize a single platform across Europe. The initial five-year agreement with MBDA will begin by moving all PCB design, schematic capture and electrical design to Zuken's modular PCB design software, CR-5000 and E<sup>3</sup>cable. The first phase will begin with implementation in France and the UK, before being incorporated in Italy and Germany.

**Routability** and **Total Board Solutions** (TBS) have partnered to develop a training course based on **Mentor Graphic's Expedition** PCB software specifically for PCB design contractors. The three-day training course is based on the EE2007.1 Expedition PCB flow. For information on the training course, visit routability.co.uk.

**Titan Global Holdings** has announced that **Titan PCB East**, a company subsidiary, has reached a definitive agreement with a management led buy-out team **Time Sensitive Circuits** (TSC) to acquire all of the assets of Titan PCB East. Denis McCarthy, an executive at Titan Electronics Group Division is the lead investor for TSC. Under the terms

## FACES

**Titan Global Holdings** has appointed **Michael Kadlec** as president and CEO of Titan Electronics. Previously a senior manager at Data Circuit Systems, Kadlec has a background in sales, marketing, and communications, and began his career in 1973. Kadlec replaced Curtis Okumura, who resigned from the company.

**Ofer Shofman**, president and CEO of **Valor Computerized Systems** has announced his retirement. Shofman is a founder of Valor, and has been president and CEO of the company for six of his fifteen years with the organization. The company has appointed **Dan Hoz** as acting president and CEO. Hoz has been the company's CFO for five years, and before that was CFO of Frontline PCB Solutions.

**CAC Inc.** and **Laminating Company of America** (LCOA) have appointed **Rocky Hilburn** as product development manager, with responsibility for marketing products for both companies. Hilburn has previously held the positions of director of marketing for Ticer Technologies, and product development manager for Gould Electronics.

**Camtek** has appointed **Roy Porat** as general manager of the company's headquarters in Israel. Porat's previous role was president of the company's Hong Kong location (Camtek HK), where he oversaw all of Camtek's activities in Asia. Aharon Sela, previously VP of sales at Camtek Europe, was appointed to replace Mr. Porat at Camtek HK.



**R&D Circuits** has appointed **Michael W. Bivens** to its sales team. Bivens will have sales responsibilities for the mountain states region, managing accounts and assisting with applications and product integration. Bivens has had previous positions with Dynamic Test Solutions as a regional account manager, as well as positions with Intel, ProbeTechnology and Microprobe.

**Milplex Circuit** of Canada has appointed **Damon DeSilva** as national sales manager. DeSilva will be responsible for all outside sales for the company, including the managing of an independent rep sales network.

## IT'S A DEAL

of the agreement, TSC will assume or repay the Titan PCB East's debt and liabilities. Closing is anticipated within thirty days, and McCarthy will manage Titan PCB East in the interim.

**Ansys, Inc.** has announced that as a result of the Security and Exchange Commission's review, it expects to finish the acquisition of Ansoft in the third quarter of 2008. The company had previously announced that the acquisition would be completed by the second quarter. When acquired, the combined companies will reportedly have over 40 sales offices and 21 development centers on three continents, and will employ approximately 1,700 people.



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## Positive Action Planning

Luck is good planning, carefully executed, with a "just do it" attitude.



**PETER  
BIGELOW**

**HAVE YOU EVER** had one of those days where it seems like nothing is going right? For some reasons it seems that everything that can go wrong does go wrong, all at once and from out of the blue. I recently had one of those four star, card carrying, absolutely miserable days.

As I tried to make sense of all that went wrong, my mind drifted back to many years ago, when I was just entering this career field. Two phrases that were bantered about in those halcyon days quickly came to mind. The first was my company's sales motivation slogan at the time, which went "Luck is good planning carefully executed!" The other phrase was the sales motivation slogan of our archrival, which went "All you really have to do is just do it!" Now, both companies were publicly traded Fortune listed companies, and these slogans were bandied about liberally at the time. Like all "young pups" just starting out with a large corporation, one of the jobs was to monitor the competition, which could include anything from how they operated to how they motivated people to make decisions. The more I think back to those days, the more I wish my career advancement could again be determined by simply monitoring high visibility activities. Equally, the more I think about those two phrases – and how important we all thought they were – I realize how the more things change, the more they stay the same.

In reality, everything you do has an element of luck attached to it. Equally, sometimes you need to, as the slogan Nike has made far more famous says, "just do it." But when those bad days come rumbling around, all I can think is that those two old slogans in combination, with the result being a streamlined interpretation like "Luck is just doing it!"

The fact that when done correctly, adopting either or both slogans can help people focus. Good planning is always essential but not always taken to heart. Planning really needs to take place at all levels in dramatic, bold ways – such as changing the focus of the company – as well as in smaller, more mundane ways, such as scheduling when a task will be performed. Nevertheless, when planning takes place everything goes more smoothly.

Execution often is where a good plan goes awry. If those involved are clueless as to what needs to take place, in proper order, by whom and with what expected result, then success becomes far less likely. And in the execution, the success of the chain is often dependent upon the weakest link, (e.g. if everyone is not on board), than all may fail.

And finally, any action is almost always better than no action. This idea is often difficult to get accepted by organiza-

tions where the concern is potential failure and who might get blamed. Still, if no one takes action, execution will not take place and the strategy will never materialize. Action is truly the catalyst to making anything happen.

This is where I drift back to my terrible day. Nothing catastrophic in itself, but put it all together, and it wasn't pretty. While often, the first thought is to take the moron(s) who made the error(s) and send them to the moon for an extended stay, when the situation is looked at objectively, it always seems to be caused by people with the best of intentions doing what they think is right to help the cause. However, because planning and execution or communication was lacking, everyone counted on luck to pull them through. Unfortunately, lady luck is not always working with you.

In fact, lady luck usually rewards those who are detail oriented and penalizes those who are not. That's where planning enters the picture. Planning is not just having a direction or goal that you are working toward, but it is considering all the things that might occur that could prevent you from successfully achieving the planned outcome. One of the items that we all seem to forget is that people need to be constantly reminded of what the goal is. As simple as it may seem, one of the things that can prevent the achievement of a goal is forgetting the original goal or plan.

Implementation requires equal attention to detail. Reminding people of what they are expected to do is part good implementation, but letting everyone know what to do if they run into a snag is also important. The last thing you want is for things to grind to a stop because no one knows what to do in an unforeseen situation that requires a decision. Those pesky details – whether in planning or implementation – always seems to make the difference between smoothly implementing a plan or a drama that makes for a terrible day.

One of the most important aspects of planning is to make sure you keep the corporation moving toward a goal. "Just doing it" requires planning to make sure everyone knows to keep moving toward the desired goal by being an integral part of the implementation process.

Finally, the real job of planning, implementing and making sure that lady luck is smiling kindly on your efforts belongs not the employees who may unintentionally throw a wrench in the works from time to time, but to the people in charge – management and supervisory people – who need to remind everyone that luck is "good planning carefully executed" and to attain it, that "all you really have to do is just do it!" **PCD&F**

**PETER BIGELOW** is president and CEO of IMI ([imipcb.com](http://imipcb.com)); [pbigelow@imipcb.com](mailto:pbigelow@imipcb.com).



# The PCB Surface Finish Universe

Or, why is immersion silver the preferred finish in ballistic missile nosecones?



**DON  
CULLEN**

**SURFACE FINISHES.** What more can be said about circuit board surface finish processes? Perhaps I'm too close to the topic, but I'm continuously bombarded by columns, publications, conferences, technical reports, press releases, and advertising on surface finishes. A portion of these are self-aggrandizing presentations of semi-scientific technical results. Others may contain nuggets of precious information. But in

the hallways of the technical conferences and at the bar before the tradeshow, you'll get the real story on surface finishes. How that OEM in Germany likes to use this surface finish, while that other assembler won't use such-and-such, ever since they got burned with that terrible failure mode. And why is immersion silver the preferred finish in ballistic missile nosecones? I guess there is always more to say about surface finishes. The proof is in the fact that people keep talking about them.

The chatter is not all technology. Pricing. Specification. Operator complaints. Document updates. Phosphorous content. Good service guys. The Japanese market. Waste water. And ...failure modes. Did I forget to mention failure modes? The list of topics continues to grow, and now the list will become a series of columns in this magazine. Our charter? To discuss all aspects of surface finishes, not just the same old boring solderability comparison charts, but the whole spectrum of hallway conversations. In this series of columns we will address printed circuit board surface finishes, a.k.a. final finishes or solderable finishes. We will keep the columns fresh, and the subjects diverse.

You may have noticed that this industry is full of technology enthusiasts (geeks). So often, we get all wrapped up in discussions of ohms and thickness distribution and surface analysis equipment. Of course, we will cover plenty of technical jargon, but we will always give the real-life applications view of the technology.

Our challenge will be in giving adequate coverage to all the various views on surface finishes.

At MacDermid, I've spent the better part of 20 years involved in surface finishes. On the lab bench, I mixed the chemicals. At the EMS site, I soldered the test vehicles. In the board shop, I suffered from "nickel itch." And back here at my desk, I've attempted to coordinate the data from all of these activities into a message to the industry. As I get older, and less able to tend to the lab bench, I'm assisted by lots of more capable people. These people will be sending in reports on specific surface finish topics as we attempt to tackle them. It's a big project, so let's get started.

Lao Tze gave us the wisdom; "The journey of a thousand miles begins with just one step." Taking that first step into the big arena of surface finishes, I plan to divide the topic into "bite-sized" units as outlined in the central figure.

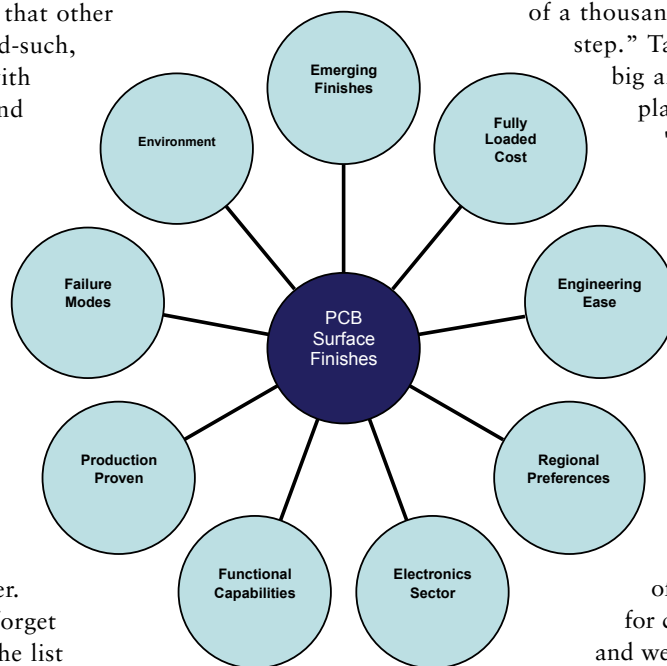
In addition, I hope you'll embrace the idea of emailing questions that can be handled in the column. Admit it, we've all complained at how information is presented in the media. (Just think about politics, nobody likes the news coverage of the presidential campaigns.)

Instead of complaining, be part of the solution! Bring us ideas for columns on surface finishing, and we'll have an honest-to-goodness debate, here in our own small world of

PCB manufacturing. On reflection, I guess I do

understand why the topic of surface finishes is so widely investigated, and why there are so many articles, conferences, etc on the topic. There is always change in board finishing technology, and there is always news in the surface finish front. I congratulate PCD&F for bringing the spotlight to surface finishes. And I hope you'll accept the responsibility for helping shape this column. You can send your questions to the magazine or directly to the columnists via the email address of the authors. **PCD&F**

**DON CULLEN** is the director - OEM and assembly applications for MacDermid, Inc. He will be a regularly featured columnist on the Final Finish Forum. He can be reached at [dpcullen@macdermid.com](mailto:dpcullen@macdermid.com).



# The Z-Direction Goes Vertical

Electronics companies across markets are hopping on PoP.



**E. JAN  
VARDAMAN**

**WHEN LAND IS LIMITED**, builders construct high-rise condos and apartments. When board real estate is limited, packages also go in the z-direction. Some of the high growth areas include stacked die CSPs and package-on-package (PoP). Next in the progression of technologies moving in three dimensions is through silicon via technology for stacking silicon devices.

**Stacked die CSPs.** Driven by portable applications that require extremely small form factors, shipments of stacked die packages have grown dramatically in the past five years. Stacked die inside CSPs are found in mobile phones and a variety of consumer products such as cameras and camcorders. More than 2.5 billion packages were shipped in 2007, and the number is expected to grow in 2008.<sup>1</sup>

While the first applications had two stacked die, the average number of die in a stack is increasing. Shipments of stacks with four or more die are common, and some companies have moved into production with stacks of six to nine die – some containing both logic and memory. Hynix has demonstrated a 20-chip memory stack in an R&D project. Typical die thicknesses in production range from 75 to 125  $\mu\text{m}$  for conventional die stacking. Stacked die are still largely wire bonded, but flip chip use is beginning to increase.

**Package-on-package.** According to Amkor, PoP is one of the company's fastest-growing packages, and may be one of the industry's, too. With almost 150 million top and 150 million bottom packages shipped last year, and an installed base of more than 150 mounting systems from a variety of companies, Amkor is probably right. Today's applications include mobile phones (the largest), digital cameras, and MP3 players. Future applications include medical products, laptops and ultra-mobile PCs. Amkor has developed a through mold via technology for next-generation PoP. It will scale with trends in the top memory package as pin counts increase, pitch transitions below 0.5 mm, and the solder balls move beyond two rows to multi rows. The new process follows a standard mold array process flow, but uses a laser to open vias (**FIGURE 1**).

Stacking die inside the package results in the thinnest package with the highest board-level reliability and lowest assembly cost compared to other z-direction packages. This package however, is not always the best choice when a logic device is added. PoP was developed because it offers several advantages over stacked die packages, especially where there is a need to stack logic and memory. Each package can be individually tested before stacking. Two packages from different suppliers can be stacked and it is easy to change memory capacity. The cost of a known good memory die may be almost the same as a packaged

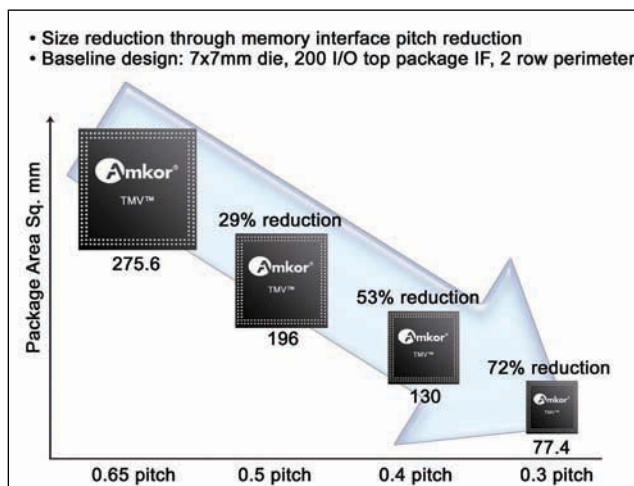
die. This can decrease the margin of the stacked die supplier. If known good die are not used, yield issues are compounded.

There are some disadvantages to PoP. Package cost may be higher for the PoP configuration than for stacked die CSP because there are two substrates rather than one.

Co-planarity of the two packages, especially during reflow, was an issue in the early days, but a tremendous amount of work has been done to alleviate this problem. Substrate warpage has been the key issue, and a number of companies have developed solutions. Both the top and bottom packages must be optimized. The liquidus/reflow temperature is the most critical in the process. Amkor has conducted extensive package warpage optimization studies varying both substrate thickness and mold materials. Substrate design rules (routing), core thickness, copper ratio and prepreg materials have been optimized. Die thickness and material properties also had to be optimized, while mold compound filler size, CTE, Tg, shrinkage and thickness had to be carefully specified. Amkor found that a very flat top package is key to good stacking yields.

Several companies, including Henkel and Indium, have introduced flux materials. Henkel's epoxy flux, for instance, shows good connectivity and increased reinforcement.<sup>2</sup>

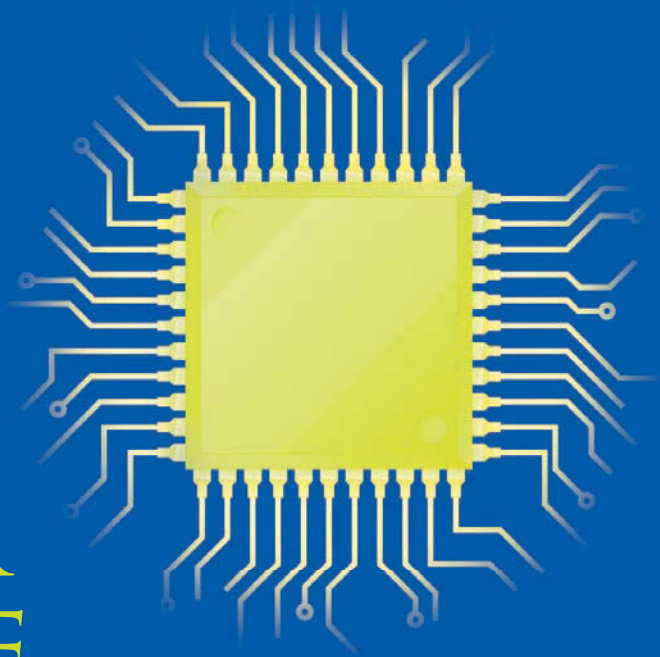
While there have been concerns over package height, which is thicker than the traditional stacked die package, solutions are being developed. These include embedding devices in the substrate, thinner substrates and concepts such as Tessera's Micro-PILR package. The top package typically contains high capacity or combo memory devices. The bottom package typically contains a high-density logic device. Body sizes range from 10 x 10



**FIGURE 1.** Size advantages using through mold via technology for memory interface density scaling in next-generation PoP. Higher performance memory architectures and smartphone size reduction requirements require bottom PoP technology that can scale in density with CSP ball/pitch density trends.

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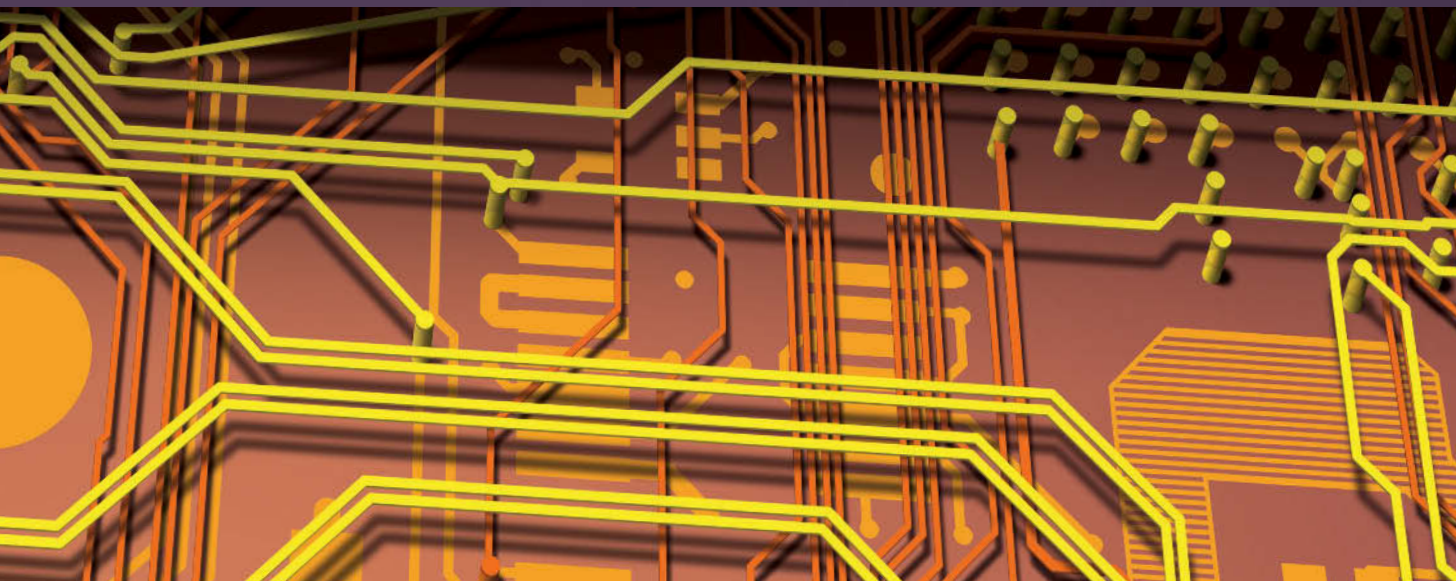
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- Two-day exhibition, featuring the industry's leading vendors
- The return of "FREE Tuesday," including six free technical sessions
- Keynote Address titled "Bringing Design to Life" by Dr. Chris Urmson, inventor of the "Boss" Chevy Tahoe
- "Designer Decision 2008," a unique session created to let designers' voices be heard
- Networking opportunities throughout the week, including the Opening Night Reception.

All show events and courses will be held at the Santa Clara Marriott—affordable luxury in the heart of the Silicon Valley. Be sure to book your room by the hotel deadline of August 25 to ensure you don't miss out on staying at the same hotel as your peers. (See page 6 for details.)

Plus, reserve your seat in the hottest classes now to ensure that you grow your knowledge in the courses you most want to take.

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*(See page 7 for conference package and discount details.)*

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# FREE SPECIAL EVENTS

## TUESDAY, SEPT. 16

### FREE TUESDAY

9 am – 7 pm in the Exhibit Hall and assigned rooms

On "FREE Tuesday," all sessions and events are free to attend! Keep reading to learn more about this year's must-attend "FREE Tuesday" technical and networking events.

### NEW! ROUNDTABLE EVENT

9 am – 11 am in Salon A/B

#### PCB Design, Fab and Assembly Roundtable: Understanding the Dynamics of the Cost/Technology Equation Across the Supply Chain

**Moderator:** Terry Heilman, Sunstone Circuits

This special roundtable discussion will provide perspectives from a range of top-level PCB manufacturers—from niche players to large multinationals. You'll:

- Enjoy open communication between partners, designers and fabricators
- Learn about typical fabrication capabilities/constraints
- Discuss tradeoffs in the fabrication process, cost drivers and yield busters, and maximizing the design process to result in an optimized final product cost
- Create a forum for continuing, constructive dialogue and an exchange of ideas

### NEW! TUESDAY KEYNOTE ADDRESS

11 am – 12 pm in Salon A/B

#### Bringing Design to Life

**Speaker:** Dr. Chris Urmson, Carnegie Mellon University

The use of semiconductors to improve all aspects of the driving experience—from safety, entertainment, navigation and even steering—is on the rise. In this exciting keynote, "Boss" inventor Dr. Chris Urmson will discuss the challenges and solutions in building such an extremely complex automobile. He will include details of the DARPA Urban Challenge, describe Boss's overall system architecture and highlight the vehicle's many component technologies. Boss is a Chevy Tahoe with more than 300,000 lines of code, capable of autonomously navigating in town and in traffic. It is equipped with more than a dozen lasers, cameras and radar systems to view the world.

*Chris Urmson is director of technology for the Urban Challenge Robotics Institute at Carnegie Mellon University. He was previously a robotics research scientist with SAIC. He developed several robotic navigation architectures and software systems currently in use by Carnegie Mellon University, NASA JPL and NASA Ames. He has made significant contributions to robot development with an emphasis on software development and system integration. He has a Ph.D. from Carnegie Mellon and a B.S. in computer engineering from the University of Manitoba.*

### EXHIBITION

12 pm – 7 pm in the Exhibit Hall

Start planning now so you'll have plenty of time to attend both days of our free two-day product and service exhibition! Visit [www.pcbwest.com](http://www.pcbwest.com) for the current list of exhibitors.

### FREE TECHNICAL SESSIONS



1 pm – 5 pm in assigned rooms

Several free technical sessions will be held on Tuesday. See page 12 of this brochure for session titles, and visit [www.pcbwest.com](http://www.pcbwest.com) for complete abstracts.

### OPENING NIGHT RECEPTION

5 pm – 7 pm in the Exhibit Hall

The Opening Night Reception will kick off at 5 pm on the show floor. This key networking event will provide you with an opportunity to meet and chat with everyone at the show—including your fellow attendees, exhibitors and speakers—in a fun, relaxed atmosphere while enjoying a selection of beverages and hearty finger foods.

### NEW! DESIGNER DECISION 2008

5:30 pm – 6:30 pm in the Exhibit Hall

**Moderator:** Kathy Nargi-Toth, Editor,

*Printed Circuit Design & Fab*

What are your most pressing design/fab concerns? In this unique one-hour session, we will open the floor to conference attendees, who are encouraged to come up with the proverbial laundry list of job- and technology-related issues and problems. The results will form the foundation of *PCD&F's* editorial coverage in 2009.

## WEDNESDAY, SEPT. 17

### EXHIBITION

10 am – 3 pm in the Exhibit Hall

The "FREE Tuesday" rush can make it difficult for exhibitors to give the personalized demonstrations that you need and want, so schedule some quality time on the second day of the Exhibition. View the current list of exhibitors at [www.pcbwest.com](http://www.pcbwest.com).

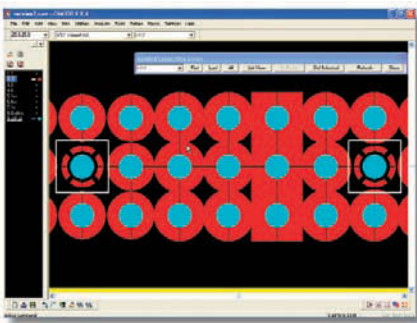


# Catch & Release.



## Build Your Boards Correctly...Hook, Line and Countersink.

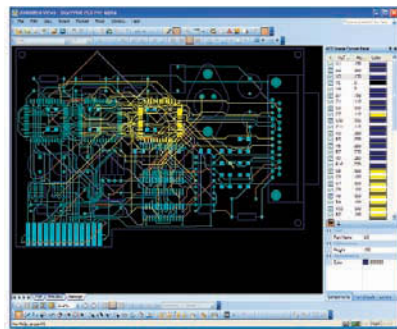
DownStream Technologies' fully integrated solutions set the standard for post-processing PCB designs. Now PCB designers can **verify, optimize, document and distribute** a comprehensive electronic Assembly Release Package, complete with all the deliverables needed for successful PCB fabrication. So don't be left reeling with PCB fabrication problems. Contact us today to find out why everything travels faster....DownStream!



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CAM350 verifies and optimizes your PCB design for more efficient PCB fabrication.

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BluePrint for PCBs automates and simplifies the process of creating PCB documentation.

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# TRAVEL INFORMATION

## Headquarters Hotel & Conference Facility

### Santa Clara Marriott

2700 Mission College Blvd  
Santa Clara, CA 95054  
(408) 988-1500

[www.marriott.com/sjcga](http://www.marriott.com/sjcga)

**Blocked Room Rate:** \$189/night

**Reservations:** 800-228-9290 or 408-988-1500

**Must Mention:** PCB West 2008

**Cut Off Date:** August 25, 2008



The Santa Clara Marriott is located in the heart of Silicon Valley, only minutes from Norman Y. Mineta San Jose International Airport and only 45 minutes from San Francisco.

- State-of-the-art, newly renovated meeting facilities, beautifully appointed guest rooms and an award winning restaurant
- All rooms include voice mail and data port, coffee maker with complimentary coffee and tea, digital On Command Video Movies, and IBAHN high-speed internet access (\$9.95)
  - Wi-fi access is available in all public areas.
  - This hotel has a smoke-free policy.
  - Area attractions include California's Great America amusement park, Winchester Mystery House and the Intel Museum.
  - Located near Intel, Cisco Systems, HP, Sun Microsystems and many other high-tech companies.

## Car Rental

Avis is the official car rental agency for PCB West 2008. Call 800-331-1600 or visit [tinyurl.com/5p9zbs](http://tinyurl.com/5p9zbs) to rent a car.

Refer to **Avis Worldwide Discount (AWD) #D900888** when making your reservation to receive our special conference rate.

## Shuttle Service

Shuttle service is not provided by the hotel.

The recommended shuttle service is:

### South & East Bay Airport Shuttle

[www.southandeastbayairportshuttle.com](http://www.southandeastbayairportshuttle.com)

## Driving Directions

**From San Jose International Airport (SJC):** Take Highway 101 North 4 miles to Great America Parkway. Exit right to Mission College Boulevard. The hotel is on the right.

**From San Francisco International Airport (SFO):** Take Highway 101 South 26 miles to Great America Parkway. Exit left to Mission College Boulevard. The hotel is on the right.

**From Oakland:** Take Highway 880 South. Exit right onto 237 West Exit Great America Parkway. Turn left onto Mission College Boulevard. The hotel is on the right.

## Airports

### San Jose International Airport (SJC)

Hotel direction: 4 miles south

Estimated taxi fare to hotel: \$17 (one way)

### San Francisco Airport (SFO)

Hotel direction: 30 miles north

Estimated taxi fare to hotel: \$90 (one way)

## Parking

**Daily Parking:** Free

**Valet Parking:** \$15 per day

**Overnight Guest Parking:** \$9 per day



# REGISTRATION INFORMATION

Register online at [www.pcbwest.com](http://www.pcbwest.com) with Priority Code #D08BD708 by August 19 and save up to \$100

## It couldn't be easier to save up to \$100 by taking advantage of our Early-Bird Discount!

Simply register by August 19, and you'll automatically receive the Early-Bird Discount prices listed below. Plus, check out the other discounts to find out if you're eligible to save even more. This year's Professional Development and 3-Day Technical Conference courses are detailed on pages 10-14. Review the course abstracts at [www.pcbwest.com](http://www.pcbwest.com). After you've checked out the program, you'll need to decide which Registration Package best fits your needs and budget. To help you make this decision, each package is described below. When you're ready to register, go to [www.pcbwest.com](http://www.pcbwest.com), and choose the registration option that applies to you (Conference or Exhibition.) Then, follow the registration system prompts.

If you have questions, call the Registration Desk at 918-496-1476.

## REGISTRATION PACKAGES

### BUILD-A-CONFERENCE PACKAGE

Choose any combination of courses even on non-sequential days. Prices are per course as shown below. This package includes your choice of courses during the entire 5-day conference, plus admission to the two-day exhibition and all of the "FREE Tuesday" and Special Events listed on page 4. Note: Alumni and Association/User Group, and Group Discounts cannot be applied to this package.

#### Type of Course

	Early-Bird Price Through 8/19	Regular Price After 8/19
Technical Conference Two-Hour Workshops (W courses), each.....	\$175	\$195
Technical Conference Half-Day Seminars (S courses), each.....	\$275	\$295
Professional Development Full-Day Tutorials (T courses), each.....	\$455	\$555
Professional Development Two-Day DEC's (DEC courses), each.....	\$845	\$945
Professional Development Three-Day DEC's (DEC course), each.....	\$1,025	\$1,125

(Note: Professional Development Tutorials and DEC courses include lunch.)

### 3-DAY TECHNICAL CONFERENCE PACKAGE

Includes your choice of courses during the entire Monday, Wednesday and Thursday 3-Day Technical Conference, plus admission to the two-day exhibition, and all of the "FREE Tuesday" and Special Events listed on page 4.

	Early-Bird Price Through 8/19	Regular Price After 8/19
3-Day Technical Conference Package.....	\$845	\$945

### 4-DAY AND 5-DAY VALUE PACKAGES

**4-day Value Package:** a terrific educational value! Includes any combination of Professional Development courses (Exception: only 1 DEC course may be taken) and 3-Day Technical Conference courses taken during four days (choose from Sun/Mon/Wed/Thu or Mon/Wed/Thu/Fri), plus admission to the two-day exhibition and all of the "FREE Tuesday" and Special Events listed on page 4. (Note: Professional Development Tutorials and DEC courses include lunch.)

	Early-Bird Price Through 8/19	Regular Price After 8/19
4-Day Value Package.....	\$1,195	\$1,295

**5-Day Value Package:** the most bang for your buck! Includes any combination of Professional Development courses (Exception: only 1 DEC course may be taken) and 3-Day Technical Conference sessions (Sun/Mon/Wed/Thu/Fri)—you decide—plus admission to the two-day exhibition and all of the "FREE Tuesday" and Special Events listed on page 4. (Note: Professional Development Tutorials and DEC courses include lunch.)

	Early-Bird Price Through 8/19	Regular Price After 8/19
5-Day Value Package.....	\$1,395	\$1,495

### EXHIBITION ONLY PACKAGE

Includes admission to the two-day exhibition and all of the "FREE Tuesday" and Special Events listed on page 4.

	Early-Bird Price Through 8/19	Regular Price After 8/19
Exhibition-Only Package.....	FREE	FREE

## DISCOUNTS

PCB West 2008 is pleased to offer the following discounts to qualifying attendees, depending on the package purchased. Except for the Early-Bird Discount, all other discounts require a Discount Code. Call the Registration Desk at 918-496-1476 to verify your eligibility and for the Discount Code prior to registering online.

**Early-Bird Discount** – Anyone who registers by August 19, 2008, will automatically receive the Early-Bird Discounts shown on this page.

#### Alumni and Association/User Group

**Discount** – Alumni of a previous UPMG PCB Show or members of a recognized industry association or user group are eligible for a discount of \$50 US on 3-Day Technical Conference, 4-Day or 5-Day Value Packages only.

**Group Discount** – Companies registering 3 or more attendees at the same time for 4-Day or 5-Day Value Packages are eligible to receive a \$100 discount per attendee, deducted from the applicable package pricing (Early-Bird or Regular). This discount may not be used in conjunction with the Alumni and Association/User Group discount. Please note: This discount is not available through online registration. Call 918-496-1476 for more information.

## REGISTRATION POLICIES

**Registration** – Complete one online registration for each registrant. Badge sharing is not allowed.

**Payment** – Payment must be made by credit card, check or Purchase Order. Registrations without complete payment information will not be processed. Credit card payments will show a charge from UP Media Group. If paying by PO, please include a \$25 US processing fee per PO in addition to the registration package fees. A signed and dated PO (with PO#) and/or full payment must be received prior to the conference in order for the attendee to be admitted into classes. For more information, call 918-496-1476.

**Refunds and Cancellations** – All refund requests must be made in writing by fax or mail to PCB West no later than August 19, 2008. Mail refund requests to: PCB West, Attn. AS, 2400 Lake Park Drive, Suite 440, Smyrna, GA 30080. Fax to 678-589-8850 or e-mail your refund or cancellation request to [askarbek@upmediagroup.com](mailto:askarbek@upmediagroup.com). "No shows" who have not made a written request by August 19, 2008, are fully liable for conference tuition/fees. Registrations made after August 19 are considered confirmed and no refund requests will be accepted; registrants will be fully liable for conference tuition/fees and will be invoiced accordingly.

**Program Changes** – The technical program of PCB West 2008 is subject to change should unforeseeable circumstances arise with respect to individual speakers. Check the PCB West Web site for the latest updates on sessions and speakers.

Early Bird Discount Deadline | Register by August 19 and save up to \$100!



# SCHEDULE-AT-A-GLANCE

## SUNDAY, SEPT. 14

**8 am – 1 pm**  
**REGISTRATION OPEN**

**9 am – 5 pm**  
**PROFESSIONAL  
DEVELOPMENT CERTIFICATE  
COURSES**

**DEC 1** – Control of Signal Integrity, EMI, Crosstalk and Grounding in High-Speed Printed Circuits

*Speaker: Rick Hartley, L-3 Communications, Avionics Systems*

**DEC 2** – PCB Design 101

*Speakers: Gary Ferrari, FTG Circuits; and Susy Webb, Fairfield Industries*

**DEC 3** – Design Challenges With HDI/Microvias, Including Hands-On Design

*Speakers: Happy Holden, Mentor Graphics; and Mike Fitts, Plexus*

**DEC 4** – EMI and EMC for the Design Engineer

*Speaker: Robert Hanson, Americom Seminars*

**NEW! T1** – Design for SMT Manufacturability From an Assembly Point of View

*Speaker: Jim Hall, ITM Consulting*

**NEW! T2** – Electrical Principles: Digital Circuits and Electrical Systems

*Speaker: Ralph Morrison, consultant*

**12 pm – 1 pm**  
**PROFESSIONAL  
DEVELOPMENT ATTENDEE  
LUNCH**

**12 pm – 10 pm**  
**PCB TOP GUN  
HALL OF FAME  
CONTEST**

## MONDAY, SEPT. 15

**8 am – 5 pm**  
**REGISTRATION OPEN**

**8 am – 7 pm**  
**PCB TOP GUN HALL OF FAME  
CONTEST**

**9 am – 5 pm**  
**PROFESSIONAL  
DEVELOPMENT CERTIFICATE  
COURSES**

**DEC 1 - DEC 4 continued**

**9 am – 11 am**  
**3-DAY TECHNICAL  
CONFERENCE COURSES**

**NEW! W1** – Choosing Components for Lead-Free (High-Temperature) Soldering

*Speaker: Vern Solberg, STC*

**NEW! W2** – Top 10 Flex Circuit Questions (and Answers)

*Speakers: Mark A. Verbrugge and Mark Finstad, Minco Products*

**9 am – 12:30 pm**  
**3-DAY TECHNICAL  
CONFERENCE COURSES**

**NEW! S1** – Traces as Transmission Lines

*Speaker: Ralph Morrison, consultant*

**NEW! S2** – Designing Out Common Failure Mechanisms

*Speaker: Jim Hall, ITM Consulting*

**12 pm – 1 pm**  
**PROFESSIONAL  
DEVELOPMENT  
ATTENDEE LUNCH**

**1:00 pm – 3 pm**  
**3-DAY TECHNICAL  
CONFERENCE COURSES**

**NEW! W3** – Which Lead-Free Solder Works Best?

*Speaker: Jasbir Bath, Flextronics*

**1:30 pm – 5 pm**  
**3-DAY TECHNICAL  
CONFERENCE COURSES**

**NEW! S3** – Design for High Density Surface Mount and Microelectronics

*Speaker: Vern Solberg, STC*

**S4** – Designing with Flex in Mind

*Speakers: Mark A. Verbrugge and Mark Finstad, Minco Products*

**NEW! S5** – Signal Integrity, Gb/s Transmission and EMI – Pulling It All Together

*Speaker: Robert Easson, Analytical Edge*

## TUESDAY, SEPT. 16

**8 am – 7 pm**  
**REGISTRATION OPEN**

**9 am – 7 pm**  
**FREE TUESDAY SESSIONS  
AND EVENTS**

**9 am – 11 am**

**NEW! RT** – PCB Design, Fab and Assembly Roundtable: Understanding the Dynamics of the Cost/Technology Equation Across the Supply Chain

*Moderator: Terry Heilman, Sunstone Circuits*

**11 am – 12 noon**

**NEW! KA – KEYNOTE  
ADDRESS**

**Bringing Design to Life**

*Speaker: Dr. Chris Urmson, Carnegie Mellon University*

**12 noon – 7 pm**  
**EXHIBITS OPEN**

**1 pm – 2 pm**  
**FREE TECHNICAL SESSIONS**

**NEW! F1** – If You Can Make It, They Can Fake It: Counterfeit Parts and China

*Speaker: Dave Ackerman, Ackerman-USA*

**NEW! F2** – Becoming a Certified Military/Aerospace Supplier

*Speaker: Steve DeWaters, Penumbra Strategies*

**2 pm – 3 pm**  
**FREE TECHNICAL SESSIONS**

**NEW! F3** – Death of a PCB Salesman

*Speaker: Greg Papandrew, Bare Board Group*

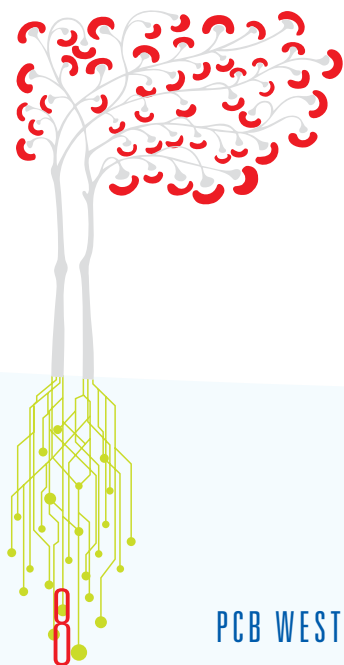
**NEW! F4** – ECAD/MCAD Collaboration

*Speaker: Larry Kenyon, Mentor Graphics*

**3 pm – 4 pm**  
**FREE TECHNICAL SESSION**

**NEW! F5** – The Effect of COTS (Commercial Off-The-Shelf) on Defense Supply Chain Integration

*Speaker: Steve DeWaters, Penumbra Strategies*



# SCHEDULE-AT-A-GLANCE

## 4 pm – 5 pm FREE TECHNICAL SESSION

**NEW! F6** – Lead-Free Cost Reductions  
*Speaker: Yash Sutariya, Saturn Electronics Corp.*

## 5 pm – 7 pm RECEPTION ON EXHIBIT FLOOR

## 5:30 pm – 6:30 pm NEW! DD – DESIGNER DECISION 2008

### WEDNESDAY, SEPT. 17

## 8 am – 4 pm REGISTRATION OPEN

## 9 am – 5 pm PROFESSIONAL DEVELOPMENT CERTIFICATE COURSE

**NEW! DEC 5** – High-Speed Design, Including Simulation Tool Use  
*Speaker: Lee Ritchey, Speeding Edge*

## 9 am – 11 am 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! W5** – Breaking New Ground in PCB RF Design  
*Speakers: Per Viklund and Loy D'Souza, Mentor Graphics*

**W6** – Designing for Asian Fabrication  
*Speaker: Happy Holden, Mentor Graphics*

**NEW! W7** – Panel Session: IC-Package-PCB Co-Design Strategies  
*Panelists: TBD*

## 9 am – 12:30 pm 3-DAY TECHNICAL CONFERENCE COURSES

**S6** – Microelectronics Design, Chip-on-Board, Flip Chip and 3D Package Technologies  
*Speaker: Vern Solberg, STC*

## 10 am - 3 pm EXHIBITS OPEN

## 11 am – 1 pm 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! W8** – Probing Signal Integrity – Measuring High-Speed Circuits  
*Speaker: Robert Easson, Analytical Edge*

## 1:30 pm – 3:30 pm 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! W9** – Panel Session: Halogen-Free Update  
*Speakers: TBD*

## 1:30 pm – 5 pm 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! S7** – Power System Design on High-Speed PCBs  
*Speaker: Rick Hartley, L-3 Communication, Avionics Systems*

**S8** – Vias and Their Effects on High-Speed Signals  
*Speaker: Robert Hanson, Americom Seminars*

**NEW! S9** – Making the Most of Your Design Time  
*Speaker: Susy Webb, Fairfield Industries*

### THURSDAY, SEPT. 18

## 8 am – 2:30 pm REGISTRATION OPEN

## 9 am – 5 pm PROFESSIONAL DEVELOPMENT CERTIFICATE COURSE

**DEC 5 continued**

## 9 am – 11 am 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! W10** – Signal Integrity Simulation Crash Course  
*Speaker: Tim Coyle, Signal Consulting Group*

**NEW! W11** – Bringing Order to the FPGA I/O Planning Madness  
*Speaker: Bruce Riggins, Taray Inc.*

## 9 am – 12:30 pm 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! S10** – Global Environmental Regulations: Updates on RoHS and WEEE, and an Intro to REACH  
*Speaker: Michael Kirschner, Design Chain Associates*

**S11** – PCB Layout Guidelines for Signal Integrity, EMI and High Speed  
*Speaker: Susy Webb, Fairfield Industries*

**S12** – Predictive Analysis for Through-Hole to HDI Conversion  
*Speaker: Gary Ferrari, FTG Circuits*

## 1:30 pm – 3:30 pm 3-DAY TECHNICAL CONFERENCE COURSES

**W12** – Materials for High Speed, High Frequency and Lead Free PCBs  
*Speaker: Rick Hartley, L-3 Communications, Avionics Systems*

**NEW! W13** – BGA Fanout Patterns  
*Speaker: Charles Pfeil, Mentor Graphics*

## 1:30 pm – 5 pm 3-DAY TECHNICAL CONFERENCE COURSES

**NEW! S13** – A PCB Designer's Guide to IBIS Models  
*Speaker: Tim Coyle, Signal Consulting Group*

**S14** – New Test Methods For High-Speed, High-Density PCBs  
*Speaker: Robert Hanson, Americom Seminars*

**S15** – The Fabrication Process: A Hands-On Experience for Designers  
*Speaker: Gary Ferrari, FTG Circuits*

### FRIDAY, SEPT. 19

## 8 am – 10 am REGISTRATION OPEN

## 9 am – 5 pm PROFESSIONAL DEVELOPMENT CERTIFICATE COURSES

**DEC 5 continued**

**T3** – Placement and Routing of Complex PCBs  
*Speaker: Rick Hartley, L-3 Communication, Avionics Systems; and Susy Webb, Fairfield Industries*

**T4** – All You Need to Know About Bypassing Including BGAs  
*Speaker: Robert Hanson, Americom Seminars*

**T5** – Basics of DFM  
*Speaker: Gary Ferrari, FTG Circuits*

## 12 pm – 1 pm PROFESSIONAL DEVELOPMENT ATTENDEE LUNCH

# PROFESSIONAL DEVELOPMENT CERTIFICATE PROGRAM

Ten courses are available in this year's Professional Development Certificate Program—one 3-day and four 2-day Design Excellence Curriculum courses (DECs) and five 1-day Tutorials (T courses). These technical courses are taught by industry experts who will provide you with the technology, theory, application and best practice information that you need to achieve professional growth and development. You'll receive a certificate of completion for each Professional Development course that you attend and complete. Note: Professional Development courses are NOT included on the Technical Conference Proceedings CD-ROM.

**SUNDAY, SEPT. 14 –  
MONDAY, SEPT. 15**

**9 am – 5 pm**

## **DEC 1 – Control of Signal Integrity, EMI, Crosstalk and Grounding in High-Speed Printed Circuits**

*Speaker: Rick Hartley, L-3 Communications, Avionics Systems*

This two-day course provides a crisp focus on the high-speed PCB and circuit design concepts needed to ensure success when utilizing the fast and ultra-fast ICs of today and tomorrow. In today's printed circuits, it's not the rate at which the circuit is clocked, rather the output edge rate (rise/fall time) of ICs that causes most signal integrity, EMI and cross talk issues. This course will cover: circuit parasitics, high-frequency currents, signal and wave propagation, time and velocity, transmission lines, proper routing technique, control of noise budgets, control of signal cross talk, power distribution and decoupling, source control of EMI, control of EMI coupling, split planes and plane islands, PCB layer stack-ups, filters and filtering techniques, system RF shielding and grounding, metal vs. plastic enclosures, slots in enclosures, and conducted EMI filters. Attendees also will learn about interfacing with the fabricator, PCB fabrication methods and concerns, PCB fabrication drawings, impedance testing and cost differential of controlled impedance PCBs.

**9 am – 5 pm**

## **DEC 2 – PCB Design 101**

*Speakers: Gary Ferrari, FTG Circuits; and Susy Webb, Fairfield Industries*

Managers often ask, "Where can I send my entry-level designers to learn the tricks of the trade?" This tutorial is the answer! Technical sessions at conferences often emphasize the latest techniques and technologies, but unfortunately those classes are usually too in-depth for the typical novice designer. This class is targeted at the entry-level PCB designer or someone just starting out in this profession.

Attendees will begin with the components and the schematic, and continue through layout and post-processing. Attendees will learn how

to interpret component specification sheets and schematics, how to plan component placement, as well as routing strategies, DFM, DFT, post-processing and more.

**9 am – 5 pm**

## **DEC 3 – Design Challenges With HDI/Microvias, Including Hands-On Design**

*Speakers: Happy Holden, Mentor Graphics; and Mike Fitts, Plexus*

Part 1 of this two-day course will examine

design techniques for the interconnection of area array components from ASIC packaging, portable products, high-performance computing and telecom to dense multichip modules. PCB design rules, materials and selection of PCB structures (blind, buried and microvias) will be examined and compared. The tutorial will define the buried passive technologies, distributed capacitance, HDI technologies, circuit routing guidelines and materials required to permit the use of widely accepted fine-pitch and BGA components. One millimeter, 0.8 mm, 0.65 mm and 0.5 mm fine-pitch components are the focus of pad, spacing and layer assignments. Channel routing techniques using blind vias will show how layers can be reduced by as much as 3X, with the associated cost reductions. Examples will be the 1,247 and 2,577 I/O 1.0 mm CCGAs. Part 2 of this two-day course is a hands-on session. It will take the principles learned in earlier in the course and apply them to real-world designs. Part 2 will begin with a discussion of CAD tool sets and include the use of an actual tool set to strengthen the understanding of how HDI can be used to solve everyday design challenges.

**9 am – 5 pm**

## **DEC 4 – EMI and EMC for the Design Engineer**

*Speaker: Robert Hanson, Americom Seminars*

If you're a PCB design engineer, it pays for you to know how and why EMI testing is conducted, as well as the typical causes of failure, even if an outside company performs your actual testing. This course offers all of the EMI information you'll need – including design considerations at CAE and CAD levels – for you to provide a compliant radiation/susceptibility product. You'll examine and identify ways to prevent common EMI/EMC problems regarding power supplies, cables, connectors, slots, discontinuity of ground planes and more. This two-day course will focus on EMI and RFI issues regarding PCBs, computers, analog designs and systems, along with relevant EMI regulations in the U.S., the European Union and Asia. Highlights include PCB radiation basics, radiation and bypass on PCBs. PCB radiation suppression techniques, grounding designs/filtering, crosstalk/termination, power and ground planes, antenna loops, spread spectrum clocking, and differential-mode and common-mode radiation.

**SUNDAY, SEPT. 14**

**9 am – 5 pm**

## **NEW! T1 – Design for SMT Manufacturability From an Assembly Point of View**

*Speaker: Jim Hall, ITM Consulting*

Providing a printed circuit design that can be cost effectively reproduced and converted into a high-quality, reliable, functional electronic product requires that the designer have a grasp of the total assembly process. In addition to designing for speed, frequency and packaging requirements, the successful designer must be knowledgeable with respect to the characteristics and capabilities of the SMT assembly process including soldering, placement, cleaning and testing. This full-day tutorial is intended to provide the participant with a broad overview of the SMT assembly processes and the design issues associated with manufacturing them. How the design effects manufacturing capability and vice versa will be

covered in depth. Equipment, processes and materials specific to the client will receive additional focus.

**9 am – 5 pm**

## **NEW! T2 – Electrical Principles: Digital Circuits and Electrical Systems**

*Speaker: Ralph Morrison, consultant*

This one-day tutorial is a review of the basic principles of electrical behavior. It covers the electric field, the magnetic field, definitions of voltage, capacitance and inductance, shielding principles, dielectrics, permeability, transformer action, Lenz's law and analog circuits. In addition, common impedance coupling, common-mode rejection, transformer shielding, energy storage in circuits, decoupling, basic transmission line theory, stripline, microstrip, buried microstrip, reflections, characteristic impedance, line matching, shorts and opens will also be discussed. Also part of the discussion will be balanced lines, ground planes, breaks in ground planes, power planes, energy stored in the ground/power plane, energy time delays, energy transport, traces jumping planes, vias, board radiation, cross coupling, ohms per square, skin effect, spectrum of waveforms, and mixing analog and digital. Lightning protection, antenna radiation, RF shielding, apertures, wave guides, reflections from conductive surfaces, absorptions, RF coupling, ESD, line filters, isolation transformers, separately derived transformers, equipment ground, isolated grounds, safety ground and screen rooms will also be reviewed.

**WEDNESDAY, SEPT. 17 –  
FRIDAY, SEPT. 19**

**9 am – 5 pm**

## **NEW! DEC 5 – High-Speed Design, Including Simulation Tool Use**

*Speaker: Lee Ritchey, Speeding Edge*

This special three-day course will cover the design of high-speed PCBs and their associated systems. It covers all the physics involved in high-speed design, explaining the science behind each one of the principles, their role in high-speed systems and how to properly manage the design process to account for them. In addition, this three-day course integrates the use of simulation for high-speed design validation. This course will give the engineering professional the fundamental knowledge necessary to make the most efficient design rule set, organize the design process to efficiently execute the design, select the appropriate PCB materials and choose the toolsets that will best suit the design process. This course is especially relevant to PCB and IC designers as device speeds outstrip the traditional packages and application notes.

**FRIDAY, SEPT. 19**

**9 am – 5 pm**

## **T3 – Placement and Routing of Complex PCBs**

*Speaker: Rick Hartley, L-3 Communication, Avionics Systems; and Susy Webb, Fairfield Industries*

The concepts behind parts placement and trace routing always seem to pique the interest of PCB designers,





# PROFESSIONAL DEVELOPMENT CERTIFICATE PROGRAM

whether new to the profession or experienced veterans of 30+ years. The reality is that there is seldom one perfect way to place parts on a PCB. However, out of the hundreds or thousands of possible variations, there usually are only a few that make sense. Understanding how to determine what those few are is the secret to placement. Once parts are placed, there are hundreds of possibilities for routing the many transmission lines of the circuit. Like placement, only a few variations really work well. Determining which placement and routing schemes optimize the design is a matter of physics, fit and opinion. This full-day tutorial will focus on both the science behind placement and routing, and the opinions of the instructor. This course will cover placement for optimum routing, placement "Rooms" (several views), and placement's effects on the schematic, EMI, board stackup, fabrication, testability, repair and assembly. It will also cover a typical design flow, routing plans, routing for best signal integrity, what's most important when routing, signals of greatest concern, I/O structures, differential pairs, analog vs. digital, and much more.

## 9 am – 5 pm

### T4 – All You Need to Know About Bypassing, Including BGAs

*Speaker: Robert Hanson, Americom Seminars*

In today's high-frequency designs, clock speeds of 1 GHz and edge rates less than 1 nsec are common. These high frequencies and their harmonics must be bypassed properly between power and ground to ensure power delivery, switching fidelity and control of radiated emissions. To ensure that the power delivery system meets its objectives, the intelligent placement, value, size and type of capacitors must be achieved. Also, at higher frequencies, the die and interplane capacitance must be optimized. Proper via placement for return current pathway minimization, laying out digital/analog interfaces, pours (Cu fills) and splits must be carefully analyzed. This full-day tutorial will illustrate a layout process that achieves 0.1 Ohm up to the knee frequency and provides methods to minimize serial/parallel resonance and achieve constant ESR.

## 9 am – 5 pm

### T5 – Basics of DFM

*Speaker: Gary Ferrari, FTG Circuits*

Lead-free, small-pitch BGAs, microvias, embedded passives, controlled impedance, EMI, what next? Each of these technologies presents manufacturing challenges that must be addressed by both today's designer, as well as any cost-reduction team. We find it easy to blame escalating costs on these

new technologies. However, much of the blame may be attributed to a lack of understanding the manufacturability rules associated with these technologies. As a designer, we should be designing for the most cost-effective product without sacrificing performance. Cost reduction, by design, forms the fundamental building blocks for this session. This full-day tutorial will be divided between lectures and interactive discussion groups. The discussion groups will explore, under guidance, material issues for lead and lead-free environments, high performance, HDI, assembly and surface finishes for various environments. The tutorial also will look at the impact of demands placed on our industry by a growing number of lead-free directives on fabrication and assembly processes. Finally, the groups will discuss new and innovative ways to test and verify a product's integrity in both current and lead-free products. There will be ample time allocated to look at individual challenges faced by attendees. Each attendee should gain a clear understanding of overall DFM issues and how they relate to current technologies, as well as lead-free directives.

# 3-DAY TECHNICAL CONFERENCE PROGRAM

The 3-Day Technical Conference consists of 28 two-hour workshops (W courses) and half-day seminars (S courses) on Monday, September 15, Wednesday, September 17 and Thursday, September 18. Tuesday, September 16 is "FREE Tuesday," a special day that provides attendees with a variety of complimentary special events and sessions, and plenty of time to visit the exhibition. The short technical courses that make up the 3-Day Technical Conference are included on the Proceedings CD-ROM provided to all conference attendees.

## MONDAY, SEPT. 15

## 9 am – 11 am

### NEW! W1 – Choosing Components for Lead-Free (High-Temperature) Soldering

*Speaker: Vern Solberg, consultant*

In compliance with RoHS, suppliers have quietly abandoned all alloy terminal plating that contains lead. Although most companies supplying finished electronic products to consumers in North America are not required by legislation to comply with RoHS, many are being forced to modify their assembly process. This is because some alloys plated on lead-free components and PCBs are not really compatible with lead-bearing materials. The other issue is the components originally developed for eutectic soldering cannot be used in a lead-free process due primarily to the mold compound's lack of capability to hold up at the elevated temperatures required for lead-free soldering. Attendees of this two-hour workshop will study and discuss potential impacts of lead-free components, review a number of component manufacturers' specifications, consider a number of compatible PCB surface finishes and better understand the assembly process variables for lead-free solder compositions currently in use. The newly published IPC-7550 standards that guide regulatory and market developments within the electronics industry will be reviewed.

## 9 am – 11 am

### NEW! W2 – Top 10 Flex Circuit Questions (and Answers)

*Speakers: Mark A. Verbrugge and Mark Finstad, Minco Products*

The world of flex circuits is an often confusing place

filled with practical and financial hazards. Remove some of the mystery by hearing the answers to the most common questions asked by circuit designers and program buyers regarding flex circuits. Culled from a combined 50 years of experience in the industry, the speakers offer a "place to start" when looking for a flex design solution.

## 9 am – 12:30 pm

### NEW! S1 – Traces as Transmission Lines

*Speaker: Ralph Morrison, consultant*

This half-day seminar on traces as transmission lines will cover characteristic impedance, trace geometries, rise and fall times, dielectrics, characteristic impedance control, matching impedances, critical lengths, reflections, mismatches, stubs, cross coupling, forward and reverse coupled waves, energy transport, the power time constant, energy management, capacitors as transmission lines, capacitor design problems, and energy storage on ICs.

## 9 am – 12:30 pm

### NEW! S2 – Designing Out Common Failure Mechanisms

*Speaker: Jim Hall, ITM Consulting*

During the course of assembly process audits and troubleshooting work, trends are seen in the types of errors and problems that occur. The resulting process problems wreak havoc with an impact on assembly yields ranging from 5 to 20%. This half-day seminar will cover common lead-free failure mechanisms and identify the "deadly sins" of surface-mount assembly, both for lead-free and "leaded" processes. We will look at feedback methodologies, DFM and assembly design issues, solder paste selection, documentation, and stencil design and tooling.

## 1 pm – 3 pm

### NEW! W3 – Which Lead-Free Solder Works Best?

*Speaker: Jasbir Bath, Flextronics*

The electronic manufacturing industry and various consortia continue to believe that the Sn -(3-4%)/Ag/(0.5-0.7%)/Cu (tin/silver/copper) alloy composition range (commonly abbreviated as SAC 305/405 alloys) will be the most widely used alloys for surface-mount solder paste in the near future. However, there is an increased and accelerated interest in several different tin-copper based alloys with additions of elements such as silver, nickel, germanium, cobalt, antimony and bismuth for lead-free wave soldering based on technical and commercial reasons. This reduction of silver content (as compared to SAC 305/405) has significant impacts in a high-solder volume consumption area such as wave soldering, where the limited supply of silver is a greater concern as compared to surface-mount reflow paste. While recognizing that the development of newer alloys is necessary for scientific and commercial progress, this two-hour workshop highlights concerns with the proliferation of lead-free wave solder alloys into mainstream production.

## 1:30 pm – 5 pm

### NEW! S3 – Design for High-Density Surface Mount and Microelectronics

*Speaker: Vern Solberg, consultant*

This half-day seminar will look at current IC packaging methodology, packaging standards, review qualification requirements, and study land pattern geometry alternatives and circuit routing guidelines, as well as important factors related to high-density PCB fabrication and assembly technologies. Topics covered

# 3-DAY TECHNICAL CONFERENCE PROGRAM

will include DFX principles; applications and standards; design guidelines for surface-mount technology and microelectronics; surface-mount land pattern development for higher density electronics; PCB materials selection and HDI fabrication methodologies; surface finish and coatings for PCB substrates; and planning for high-volume automated assembly processing.

**1:30 pm – 5 pm**

## **S4 – Designing with Flex in Mind**

*Speakers: Mark A. Verbrugge and Mark Finstad, Minco Products*

Flexible circuitry is more than just an electrical interconnect. Since a flexible circuit is required to bend and flex during and after installation, it becomes as much a mechanical device as an electrical device. A robust flexible circuit design goes much deeper than just connecting the nets. Small variations in materials selection, materials stackup, and routing features can dictate whether a flex circuit will function for years or fail within minutes. This half-day seminar will examine the electrical and mechanical features that must be incorporated into the design, and how those features will interact. The course also will cover how to select the proper materials and stack up, routing techniques, termination variety and options to make the product more rugged. Emphasis will be placed on common design errors and cost drivers. We will review the design process from first concept to the finished flex circuit. We also will explore when and where to use a flex circuit, when to choose a rigid-flex over a standard multilayer, all while maximizing value for the lowest total cost of ownership.

**1:30 pm – 5 pm**

## **NEW! S5 – Signal Integrity, Gb/s Transmission and EMI – Pulling It All Together**

*Speaker: Robert Easson, Analytical Edge*

Digital design engineers and PCB layout designers conventionally think in terms of signal voltages changing with time, whereas EMC engineers tend to work with currents and frequencies. Furthermore, the move to multi-Gb/s serial transmission on PCBs has introduced further concepts such as BER (bit error ratio), ISI (inter-symbol interference) and eye patterns, and much more emphasis is on the high-frequency properties of PCB laminates. This half-day seminar aims to relate all these requirements to high-speed PCB layout in a way that is understandable for PCB layout designers and engineers who are not RF (radio frequency) experts. The key that connects these issues is the relationship between signal rise time and circuit bandwidth. Attendees will learn how to relate rise time, bandwidth and clock frequency (without the use of advanced math), and how this provides insight into the complex behavior of capacitance, inductance and resonance in PCBs and components. This is applied directly to key areas of high-speed design to aid in understanding power distribution, inductance in the circuit path, coupling, crosstalk and discontinuities on transmission lines. Applying these concepts to PCB laminate properties shows how ISI develops and degrades eye patterns and BER. Attendees will also gain insight into EMC concerns of differential and common mode impedance and radiation, ground loops and grounding principles.

## TUESDAY, SEPT. 16

**IT'S FREE TUESDAY! All Tuesday events and technical sessions are FREE to all conference and exhibition attendees. These courses are not part of the 3-Day Technical Conference.**

**1 pm – 2 pm**

## **NEW! F1 – If You Can Make It, They Can Fake It: Counterfeit Parts and China**

*Speaker: David Ackerman, Ackerman-USA*

According to the International Chamber of Commerce Counterfeiting Intelligence Bureau, counterfeit product represents as much as 7% of total world trade – that translates to more than \$550 billion in lost revenues for legitimate companies annually. This free session will focus on what you need to know to minimize this problem for your business; how to detect counterfeit parts, how to conduct in-house testing and how to utilize third-party testing houses. The session also will give you guidance on how to be a proactive buyer and to know who you're buying from. You will learn about the efforts being made to overcome this counterfeit problem, and how you can be involved. In short, you will learn how to recognize the problem, minimize risk and become part of the solution!

**1 pm – 2 pm**

## **NEW! F2 – Becoming a Certified Military/Aerospace Supplier**

*Speaker: Steve DeWaters, Penumbra Strategies*

By its very nature, the military/aerospace sector is largely insulated and has highly specific criteria for any supplier wishing to enter and sustain business within its community. It is critical to understand which programs are viable, which contractors to contact (and how), as well as to understand the criteria for involvement. Military program research from known, credible analyst communities is a rich trove that can provide actionable, immediate information for the business development manager (BDM) to penetrate the marketplace. The "10,000 foot view" of the markets is interesting but insufficient to target, acquire and engage decisionmakers. Similarly, lead lists are only as good as the business intelligence behind them. The name of the game for the BDM is business development, preferably along the smartest, shortest path-to-market. This free session is geared toward identifying credible sources and methods for using market research to expedite the business development process.

**2 pm – 3 pm**

## **NEW! F3 – Death of a PCB Salesman**

*Speaker: Greg Papandrew, Bare Board Group*

Domestic PCB salesmen are getting hit by a lot of flak in the today's global market, and it is not because of China. They are being hit by friendly fire! North American PCB manufacturers have overlooked the importance of maintaining a proper sales force, and in doing so, they are killing their own business. Forget fancy plating tanks, drill machines and new technologies. The PCB business needs to develop better services and marketing plans, and it needs to focus on building stronger customer relationships. Covering topics that are crucial to the circuit board industry, this free session is packed with marketing wisdom that PCB salesmen, sales managers and owners of board manufacturing companies can use to make a lasting impact on their business and on their careers. These are not quick fixes. They are real, long-term solutions to long-term problems.

**2 pm – 3 pm**

## **NEW! F4 – ECAD/MCAD Collaboration**

*Speaker: Larry Kenyon, Mentor Graphics*

ECAD/MCAD engineers must communicate regularly to ensure that their designs do not impinge on their counterparts' requirements or constraints. This is often done through verbal or e-mail communication, complicated when the two organizations are not in the same location, time zone or even country. Occasionally, this inefficiency results in missed schedules and problematic design conflicts, which in turn, results in increased costs. Technology has been developed to provide an ECAD/MCAD collaboration environment to alleviate this problem. Using this technology, ECAD and MCAD teams can work in their own environments, each with 3-D viewing capabilities, to discuss and analyze proposed changes as they happen, in real time. The ability to iterate cooperatively over small design iterations, rather than the larger iterations that traditionally have caused major re-designs, has the potential to eliminate surprises that result in increased costs and missed schedules.

**3 pm – 4 pm**

## **NEW! F5 – The Effect of COTS (Commercial Off-The-Shelf) on Defense Supply Chain Integration**

*Speaker: Steve DeWaters, Penumbra Strategies*

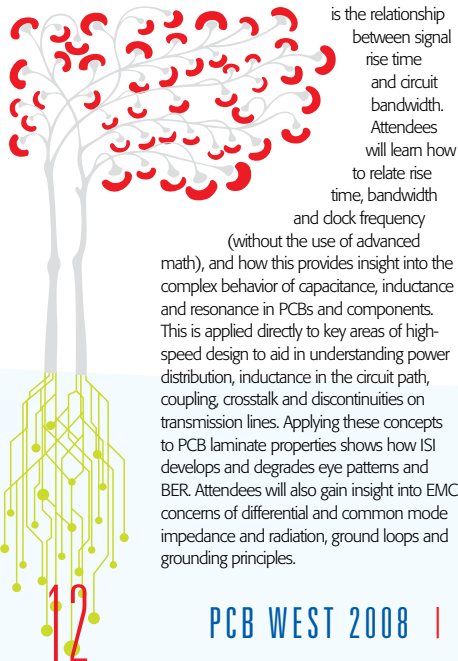
With the advent of the now famous "Perry Memo" [Specifications & Standards – A New Way of Doing Business], DTD 29 Jun 94, commercial solutions began entering into military designs. These solutions (COTS) opened up the possibility that integrating commercial and military development/manufacturing facilitates dual-use processes and products, and contributes to an expanded industrial base that is capable of meeting defense needs at lower costs. To date, there have been many successful applications, but many more have failed. Understanding the demands and commercial limits opens a realm of opportunities for commercial suppliers to address. The military/industrial complex is a unique culture with expectations that are often out-of-synch with commercial mentalities. Learning more about the adoption rate of COTS – which applications, which programs – can help commercial suppliers steer their development and marketing efforts. This free session will provide the attendee with a COTS overview; successful applications; unsuccessful applications; and the limitations and opportunities.

**4 pm – 5 pm**

## **NEW! F6 – Lead-Free Cost Reductions**

*Speaker: Yash Sutariya, Saturn Electronics*

Focusing on the implementation of necessary changes, this presentation supplies immediate results by reducing lead-free costs via the use of recently-introduced, proven materials and finishes. "The transition to lead-free is now all but standard. We've all made it. But Saturn, one of the leading voices in that transition, is now ready to share its refined cost-reducing methods," says Yash Sutariya, VP of Saturn. The presentation will instruct attendees on controlling the process, choosing the right materials and establishing the proper guidelines.



# 3-DAY TECHNICAL CONFERENCE PROGRAM

## WEDNESDAY, SEPT. 17

### 9 am – 11 am

#### **NEW! W5 – Breaking New Ground in PCB RF Design**

*Speakers: Per Viklund and Loy Dz'Souza, Mentor Graphics*

Designing mixed analog-digital PCBs requires considerably more effort than single-signal PCBs. Crosstalk between signals must be avoided, and analog circuits can be susceptible to the EMI generated by high-speed digital circuits. Stepping beyond that and including RF signals with analog and digital on the same PCB induces even more issues that must be properly dealt with. With the increasing number of wireless products infiltrating the market, PCB designs that place all three types of circuits on a single board are becoming more and more common. This two-hour workshop identifies many of the issues, and presents solutions and design considerations for mixed-RF/analog/digital PCB designs.

### 9 am – 11 am

#### **W6 – Designing for Asian Fabrication**

*Speaker: Happy Holden, Mentor Graphics*

If there were ever a time to have a full understanding of DFM, then having your boards built in China is that time! This workshop will highlight the issues, choices, alternatives and conditions that designers need to consider in order to make a PCB manufacturable in Asia, especially China. Attendees will learn how to determine if a fabricator is capable of handling an order; how to use IPC-9151 capability benchmarking to select fabricators; when to control impedance; plating, finishes and thickness distribution; mechanical and image tolerances; materials, multilayer stackup and hole plugging; thieving, plating concerns and why plating thickness varies; calculations vs. 2-D field solvers; and much more.

### 9 am – 11 am

#### **NEW! W7 – Panel Session: IC-Package-PCB Co-Design Strategies**

*Panelists: TBD*

The electronics industry is poised on the brink of major changes in the way we approach system design. SoC devices and SiPs need design teams comprised of members from all disciplines; chip, package and board designers need to cooperate to bring a successful design to completion. Concurrent co-design methodologies, supported by collaborative software systems, are making way for fundamental changes that will impact the basic roles of engineer and circuit designer in the future. Through a number of case study examples, this two-hour panel session will highlight the current changes in electronic system design that will impact your design future.

### 9 am – 12:30 pm

#### **S6 – Microelectronics Design, Chip-on-Board, Flip Chip and 3-D Package Technologies**

*Speaker: Vern Solberg, consultant*

As new generations of electronics products emerge, they often surpass the capability of existing packaging and interconnection technology and the infrastructure needed to support newer technologies. This movement is occurring at all levels: the IC, the IC package, the module, the hybrid, and the PCB, which ties all the systems together. Interconnection density and methodology become the measure of successfully managing performance. The gap

between PCBs and semiconductor technology (wafer-level integration) is greater than one order of magnitude in interconnection density capability, although the development of fine-pitch substrates and assembly technology has narrowed the gap somewhat. All viable efforts are being used in filling this void utilizing uncased ICs (flip-chips and incorporating more than one die or more than one part in the assembly process. This half-day seminar provides a comparison of different commonly used technologies, including flip-chip, chip-size, wafer-level and 3-D array package methodologies detailed in a new publication, IPC-7094. It considers the effect of bare die or die-size components in an uncased or minimally cased format, and the impact on current component characteristics, and reviews the appropriate PCB design guidelines to ensure efficient assembly processing. The focus of the IPC document is to provide useful and practical information to those who are mounting bare die or die-size array components or who are considering the adoption of miniature IC package technology.

### 11 am – 1 pm

#### **NEW! W8 – Probing Signal Integrity – Measuring High-Speed Circuits**

*Speaker: Robert Easson, Analytical Edge*

Engineers and technicians traditionally rely on oscilloscopes and logic analyzers to test digital PCBs. With many IC output drivers now having sub-nanosecond rise times, routine oscilloscope measurements to test digital PCBs may be inadequate to resolve high-speed design issues. Other measurement instruments such as the time domain reflectometer (TDR) and vector network analyzer (VNA) may provide more meaningful information. In addition, Gb/s serial transmission brings a new set of measurement requirements such as BER (bit error ratio), ISI (inter-symbol interference) and eye patterns. This two-hour workshop looks at what needs to be measured on a PCB (signals and system paths) and how well they can be measured (as a function of time or frequency). Beginning with a review of TDR, VNA and oscilloscope measurements (explained in simple terms of voltage, current and reflection), attendees will gain insight into the benefits and limitations of each technique from a high-speed design standpoint. Attendees will also learn how to assess the measurement bandwidths required for accurate signal measurement, how circuit probes degrade measurements, and how to choose what techniques may work best in specific situations. BER, ISI and S-parameter measurements are included in this tutorial

### 1:30 pm – 3:30 pm

#### **NEW! W9 – Panel Session: Halogen-Free Update**

*Speakers: TBD*

Why halogen-free? The question was raised more than 20 years ago and the debate continues. What are the advantages to eliminating halogen from the electronics supply chain? Is the proposal based on science? Or a knee-jerk response to a misguided ideal? With the rapid changes in the regulatory positions on specific bromine materials, the requirement to move toward supposedly "greener" halogen-free laminates is faltering. No law exists to push acceptance of these halogen-free materials forward and it seems clear that specific efforts to push for a removal of bromine from laminate materials is losing ground. We have invited experts in the area of halogen-free electronics to present current global positions on the topic. Expect an informative discussion and spirited debate at this two-hour panel session.

### 1:30 pm – 5 pm

#### **NEW! S7 – Power System Design on High-Speed PCBs**

*Speaker: Rick Hartley, L-3 Communication, Avionics Systems*

The power distribution section of a PCB is the foundation around which all things work in the circuit. If this is not designed correctly, the entire circuit is at risk from noise, to say nothing of the severely increased possibilities for EMI. Low impedance in the power bus across the range of harmonic frequencies of a digital circuit is critical. This half-day seminar will cover the major components of the power bus, the power distribution path, medium- and high-frequency decoupling concerns, the importance of IC pin assignments, placement of decoupling, real performance of capacitors (verses myth), how much decoupling is enough, why use one value of capacitor, anti-resonant peaks, the importance and performance of power/ground planes and the importance of board stack.

### 1:30 pm – 5 pm

#### **S8 – Vias and Their Effects on High-Speed Signals**

*Speaker: Robert Hanson, Americom Seminars*

Vias are much more than holes; they can have a profound effect on your digital signal. This half-day seminar will cover the mechanical properties of vias – from drilling and plating, to lamination, electrolysis and electroplating. Attendees will learn about capacitance and inductance of vias; return current and its relation to vias; through-hole, blind, buried and microvias; methods for drilling; aspect ratios; and cost tradeoffs. Discussion will focus on whether vias and autorouters are HDI compatible, via discontinuity and via resonance concerns, capacitance and inductance of vias (through-hole, blind, buried), eliminating reflections of vias, and return current and intelligent via placement.

### 1:30 pm – 5 pm

#### **NEW! S9 – Making the Most of Your Design Time**

*Speaker: Susy Webb, Fairfield Industries*

Layout time is often one of the last things considered in the project cycle, so designers need to manage their time wisely to get the job done. This half-day seminar will discuss ways to do that from many angles of the design. We will discuss: streamlining the input and output processes; fully utilizing the software including using macros and scripts; optimizing the design preparation and layout; and making the checking, saving and ECO processes more manageable.



# 3-DAY TECHNICAL CONFERENCE PROGRAM

## THURSDAY, SEPT. 18

### 9 am – 11 am

#### **NEW! W10 – Signal-Integrity Simulation Crash Course**

*Speaker: Tim Coyle, Signal Consulting Group*

As complexity increases with every new design, the need to simulate an interface to identify acceptable routing topologies becomes even more apparent. While the prospect of setting up a signal-integrity simulation environment can be daunting, with the right understanding of the fundamentals, an interface can be simulated with minimal effort. For PCB designers who are not familiar with setting up a signal-integrity simulation, this two-hour workshop will address the basic building blocks of a signal-integrity simulation that will allow for successful prototyping. A sample DDR3 interface in a DIMM configuration will be used to show the progression of setting up a simulation environment and finding a solution space for a design parameter.

### 9 am – 11 am

#### **NEW! W11 – Bringing Order to the FPGA I/O Planning Madness**

*Speaker: Bruce Riggins, Taray*

With their zero NRE (non-recurring engineering) and shorter design cycles, FPGAs are increasingly replacing ASICs in mainstream products. Higher pin densities leads to increased routing congestion as more and more signals converge into a smaller and smaller space on the PCB. Design teams struggle with effectively choosing I/O pin assignments that not only work well for the FPGA but that are optimized for the PCB routing. Lacking sufficient EDA commercial tools to deal with the issue, many companies attempt to roll their own solutions. This two-hour workshop will present a solution to the FPGA I/O assignment crisis, describing ways of viewing the FPGA design-in effort from a system-level perspective. We will discuss why moving the PCB layout process earlier in the design cycle is imperative and show the benefits that this approach brings. We will also talk about the need to consider the problem from a physical, electrical and logical standpoint. Finally, we will consider the schematic and ECO processes and propose superior solutions and alternatives to dealing with the difficulties caused by FPGA pin assignment changes.

### 9 am – 12:30 pm

#### **NEW! S10 – Global Environmental**

**Regulations:  
Updates  
on RoHS  
and  
WEEE,  
and an  
Intro to  
REACH**

*Speaker: Michael Kirschner, Design Chain Associates*

RoHS and WEEE in the European Union are both going through review cycles, and we're in the midst of the first major compliance activities for REACH (Registration, Evaluation, Authorization, and Restriction of Chemicals). This half-day seminar will provide you with an update on RoHS and WEEE, then spend the bulk of the time on REACH. We will describe what it is, how it impacts electrical and electronic products and supply chains, and what companies need to do to comply as well as identify and mitigate risk. We will also take a look

at upcoming issues and challenges to our industry and others.

### 9 am – 12:30 pm

#### **S11 – PCB Layout Guidelines for Signal Integrity, EMI and High Speed**

*Speaker: Susy Webb, Fairfield Industries*

This half-day seminar will provide guidelines for designers to incorporate the complex physics and electronics behind signal integrity, EMI and high-speed design into actual board design. We will start with electronics basics and why understanding the concepts is important for board layout. We will then discuss incorporating signal integrity and EMI issues into successful board designs. Last, we will illustrate good practices for high-speed board design including placement, stackup, planes, routing and more.

### 9 am – 12:30 pm

#### **S12 – Predictive Analysis for Through-Hole to HDI Conversion**

*Speaker: Gary Ferrari, FTG Circuits*

Designers are often faced with the challenge to estimate how many conductive layers a particular board design would require. We use our best experiences to come up with an estimate, but it's only an estimate. How many times have we run out of routing channels only to have to add an additional layer pair? It worsens if we have to continue adding layer pairs until the design is complete, and it becomes a complete disaster if we have to resort to HDI at the end to complete the project. This half-day seminar looks at variables that are analyzed to predict routing requirements of a design, as well as alternative HDI structures. Design rules, performance gains and cost comparisons highlight this session. The attendee should gain a clear understanding of what critical identifiers will lead them to an HDI design, which is a more cost effective alternative than adding additional layers to a current through-hole design, as well as the improved performance gained.

### 1:30 pm – 3:30 pm

#### **W12 – Materials for High-Speed, High-Frequency and Lead-Free PCBs**

*Speaker: Rick Hartley, L-3 Communications, Avionics Systems*

In a high-speed or high-frequency circuit, performance is dependent upon a number of characteristics and variables, which all accumulate to affect the noise budget of the circuit. Several of these issues are driven by the PCB's base material characteristics. At high frequencies, materials can and do have a profound impact on performance. This two-hour workshop will discuss the base materials commonly used in high-speed digital and high-frequency analog circuits (including FR4), looking at their advantages and disadvantages. It will also detail how to calculate their impact on circuit performance, hence how to choose a cost-effective material for any specific application. Finally, we will also look at how each of these materials fits into today's lead-free products.

### 1:30 pm – 3:30 pm

#### **NEW! W13 – BGA Fanout Patterns**

*Speaker: Charles Pfeil, Mentor Graphics*

Choosing the appropriate fanout patterns for routing BGAs can enable fewer layers and better signal integrity. When using HDI, many options are available for fanout patterns. This two-hour workshop demonstrates different fanout patterns in the context of HDI stackups and how they can be successfully applied on large dense BGAs.

### 1:30 pm – 5 pm

#### **NEW! S13 – A PCB Designer's Guide to IBIS Models**

*Speaker: Tim Coyle, Signal Consulting Group*

Simulating a PCB design gives a board designer insight into potential signal integrity issues such as overshoot and setup/hold margin. Using IBIS models to represent the I/O device is a common industry practice to allow fast simulations and is widely supported by most PCB environments and chip vendors. This half-day seminar will cover the basics of IBIS modeling from what they model to how they are generated. We will also discuss how to validate an IBIS model and some tips and tricks to fixing poor quality IBIS models. This will teach designers basic theory behind IBIS models, the process to generate an IBIS model and how to fix an IBIS model.

### 1:30 pm – 5 pm

#### **S14 – New Test Methods For High-Speed, High-Density PCBs**

*Speaker: Robert Hanson, Americom Seminars*

Due to high-speed, stackup restrictions, blind/buried vias and many other limitations, traditional test methods may not provide the capabilities to test today's high-speed, high-frequency PCBs. This half-day seminar will explain why traditional test methods – i.e., clamshell fixtures for bare board testing to detect opens/shorts, MDA and ICT for fault detection/fault isolation on the production line and functional test using rack and stack hardware at the operational level – are losing applicability. This course also will define new methods of test that confront the restrictions and, in turn, provide cost-effective solutions. Attendees will learn much more, including: What is microsectioning testing and what will it accomplish when testing blind and buried vias? Why is vision testing (AOI, X-ray, laser) becoming more popular for testing blind vias? Why is flying probe (F/P) and vision being used at receiving/inspection (R/I)? What test strategies dictate using either test at R/I? How do we use new F/P techniques in lieu of TDR or VNA? How do we conduct Zo test at bare board using TDR or VNA? How do we test when the via/pad can't be contacted using traditional ICT/MDA BON techniques? What is bead probe testing, and why is it the hottest topic for an emerging new test strategy?

### 1:30 pm – 5 pm

#### **S15 – The Fabrication Process: A Hands-On Experience for Designers**

*Speaker: Gary Ferrari, FTG Circuits*

PCBs have evolved over the years into quite complex components utilizing blind and buried vias, embedded components, impedance, etc. A daunting set of design rules is associated with these advances. However, to fully understand and utilize these new requirements, the modern PCB designer must grasp the basics, or foundation, of the processes used to fabricate a high-tech PCB. This highly interactive half-day seminar will cover the basic manufacturing steps while highlighting those areas and the rules associated with them of most concern to the PCB designer. Covered processes include double sided, multilayer, HDI, and blind and buried vias to name a few. The attendee should come out of this course with a clear understanding of the overall PCB fabrication process and how it affects the design process.



# SPEAKER BIOGRAPHIES

**TIM COYLE** is a principal consultant and owner of Signal Consulting Group LLC, which provides consulting and training for high-speed digital designs.

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**LARRY KENYON** has worked in many facets of the electronics industry, including PCB assembly, test and final assembly. The breadth of background

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**PER VIKLUND** is director of IC packaging and RF at Mentor Graphics. He has over 25 years' experience in system, RF and package mixed-technology design.

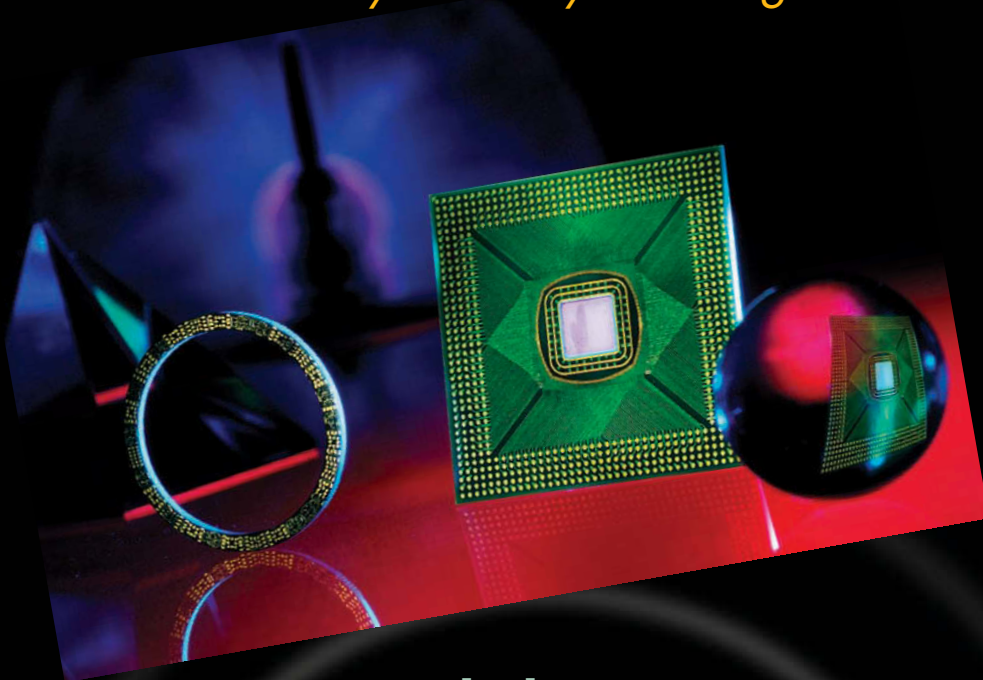
**SUSY WEBB** is a senior PCB designer with 28 years of design experience. She has worked in a variety of fields, including point-to-point microwave network systems, oceanographic oil exploration equipment, and CPCI and ATX computer motherboards. Webb is CID certified and is an active member of the IPC Designers Council, currently working as a member of its national executive board, high-speed and education committees.

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mm to 15 x 15 mm, with bottom-side ball counts ranging from 240 to more than 400, and package interconnect ball counts ranging from 104 to 160.<sup>3</sup>

To achieve small package bodies, an increasing number of companies use flip chip inside the package, especially for the bottom die in a package of a PoP. Flip chip reduces pitch for the top package of a PoP, and improves electrical performance for devices such as baseband processors by delivering power directly to the processor core, along with reduced IR drop and reduced EMI.

**TSV: The ultimate in 3-D.** TSV technology permits devices to be placed and wired in the third dimension. 3-D TSV adoption promises higher clock rates, lower power dissipation and higher integration density. The technology will be adopted in many applications because it solves issues related to electrical performance, memory latency, power, and noise on and off the chip. For some applications, a high-bandwidth memory interface to the logic has been the main driver for the technology's development. Both logic and memory device applications are expected to begin within a few years. The addition of DSP to image sensors is also anticipated in future camera module versions. There were more than three dozen papers on 3-D packaging at the Electronic Components and Technology Conference in May 27-30, and the sessions were packed.

Even with 3-D ICs' advantages, there are several challenges to the adoption of 3-D architectures. These challenges need to be overcome for the technology to see widespread adoption.

- Commercial availability of EDA tools and design methodologies.
- Thermal concerns due to increased power densities.
- Test, especially for repartitioned logic.

The TSV market will be established when the benefits justify the cost, and on a case-by-case basis. While through vias are used in image sensors for camera modules today, other applications will take time. TSMC's recent TSV announcements as part of its Open Innovation Platform will aid the adoption. TSMC is working with customers on design software and has introduced a SPIC tool design kit. The first technology is a post through-silicon via technology capable of 140  $\mu\text{m}$  pitch. By the end of 2009, TSMC will offer a post TSV technology with 60  $\mu\text{m}$  pitch and, sometime in 2011, 17  $\mu\text{m}$  pitch inline capability.

Movement in the z-direction continues and a variety of solutions will remain. Stacked die CSPs will continue to see high growth. PoP adoption will expand as many system makers hop on the bandwagon. The ultimate silicon stacking, 3-D TSV, will see widespread adoption as some of today's key issues are resolved. **PCD&F**

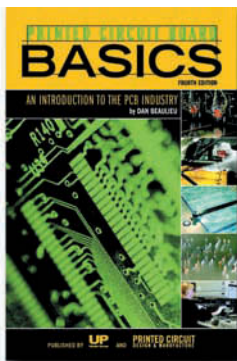
## REFERENCES

1. TechSearch International Inc., *Advanced Packaging Update: Market and Technology Trends*, March 2008.
2. B. Toleno Ph.D., and D. Maslyk, "Process and Assembly Methods for Increased Yield of Package On Package Devices," IPC Apex Proceedings, April 2008.

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## Electrodeposition of Copper, Part 2

Advanced technology PCBs require electrolytic copper capable of excellent throwing power and leveling.



**MICHAEL  
CARANO**

**WITH SMALLER DIAMETER** vias and thicker panels, the importance of a high throwing power, high leveling acid copper electrodeposition process takes on added significance. In order for high aspect ratio vias to withstand multiple thermal cycles, the copper plating within the via must be uniform and have optimum physical properties. Additionally, the quality of the copper deposit

depends in part on the performance of the initial metallization process that has been previously discussed.

### Mathematical Modeling of Plating Uniformity

There are a number of published studies on the subject of plating uniformity in through holes. In these studies, researchers developed models to test plating uniformity. With respect to plated through holes, the models attempted to predict what influence key variables had on plating uniformity. The variables include:

- Mass Transport
- Ohmic resistance
- Electrode reactions
- Circuitry layout

Basically, one has to optimize the electrolytic copper process for plating on the surface and in the through hole. Studies indicated that ohmic resistance tended to dominate the plating process with the high-

er aspect ratio through holes. For example, the ohmic resistance (or voltage drop) can be explained by the following model:

$$E = \frac{JL^2}{2Kd} \quad \text{Eq. 1}$$

Where E is the ohmic resistance, J is cathode current density, K is solution resistance, d is hole diameter and L is length of hole (board thickness).

As the model shows, the thickness of the panel or length of the hole influences the difficulty of plating by a squared term. In addition, an optimal balance between agitation on the PCB surface and solution movement in the holes was required to achieve a compromise between uniform plating distribution across the panel surface and excellent throwing power in the hole. The model developed by these scientists has been verified time and time again.

Plating uniformity is a continual challenge for through-hole PCB manufacturing and is becoming more difficult with increasingly complex designs. It should be quite clear that plating uniformity is closely influenced by solution chemistry and solution agitation conditions.

Certainly, understanding the ramifications of the model is critical with respect to plating distribution, throwing power and overall plated through-hole reliability. The factors listed in the fishbone diagram below provide a framework for discussion. These and other variables will be discussed in this and subsequent columns. The fishbone diagram in **FIGURE 1** highlight the numerous interactions that occur during the electrolytic copper plating process.

The function of the basic chemical components in an electrolytic copper bath are listed below:

**Copper Sulfate.** Provides source of copper (+2) ions.

**Sulfuric Acid.** Provides solution conductivity and anode corrosion.

**Chloride Ion.** Plays a synergistic role with organic additives in the brightening and leveling mechanism. Also promotes even anode corrosion.

**Organic Addition Agents.** There are a myriad of addition agents commercially available. The function of these additives is to provide a mechanism whereby the copper deposit is plated in a level and ductile condition. Typically, the addition agent package consists of grain refiners, leveling agents and suppressors. For purposes of this discussion, the grain refiner is used interchangeably with the term “brightener.”



**FIGURE 1.** The fishbone diagram outlines the interactions that occur during the electrolytic copper plating process.

**Brightener.** The brightener or grain refiner is a member of a class of organic compounds characterized by the designation X-S. The grain refiner contains low molecular weight sulphur (S) and a second atom (X) of high polarity and/or ionic character. Typical brightener additives are thiourea, disulfides, thiocarbamates, thiocarboxylic acid amides, etc. The “brightener,” by coulombic attraction, forms a layer on the surface where the additive assists in the refinement of the copper grain structure as it is deposited. The structure of the copper deposit is often described as fine grained or amorphous.

**Suppressors.** Another component of the acid copper addition agent system will be high molecular weight polyether compounds, surfactants, polyoxalkylene glycols, and others of similar structure. This additive acts as a suppressor by converting an unevenly distributed stationary cathode diffusion layer into a more evenly distributed layer. This action reduces the variation in copper deposit thickness across the surface caused by uneven diffusion paths that exist in the absence of a suppressor. In other words, the sup-

pressor acts to prevent overplating in the high current density areas of the printed circuit board.

**Leveler.** A third component of the additive system is referred to as a leveler. The leveler is highly polar, and by its nature adsorbs preferentially near the most negatively charged sites of the cathode (PCB). This action slows down the charge transfer of the copper ions to copper metal, thus slowing down the plating rate in those areas typically considered high current density areas. Basically, if over plating distribution and throwing power is to be improved, this is a necessary action.

In the next installment of Positive Plating, we will look further into the electrochemistry of plating using the various mathematical models for determining plating uniformity. **PCD&F**

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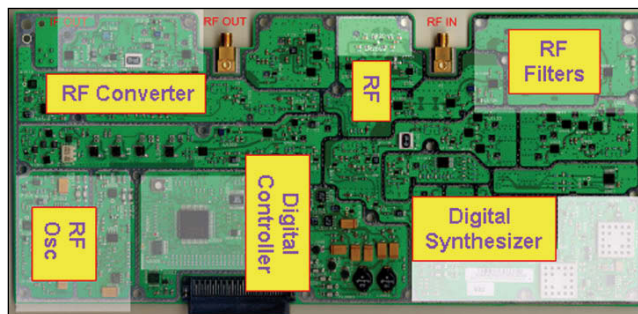
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# The COST of ADVANCING TECHNOLOGY

New collaborative systems connect designers and extend their reach beyond the PCB to other disciplines, enhancing the product development cycle. **by HENRY POTTS**

Dramatic changes have affected the electronics industry in the past few years and changes continue. Competition is steeper. Emerging countries once known for inexpensive manufacturing are now mainstream suppliers of high-end competitive products. Electronic companies once vertically organized from design through manufacturing now find themselves not only outsourcing manufacturing but also portions of their product design. PCB fabrication technologies are rapidly advancing. All of this puts companies on steep learning, technology adoption, and re-organization curves that require the use of more sophisticated and costly EDA design solutions. Such is the price of staying competitive.

Regardless of the industry segment (telecom, consumer, automotive, industrial, and even military and aerospace), there are common business needs expressed by all electronics companies as they strive to survive. The first need is to meet ever decreasing time-to-market goals. Especially important in the consumer industry where product life cycles are measured in months, the company's ability to hit a short market window and charge premium pricing for their new product makes the difference between profit and loss. Witness the

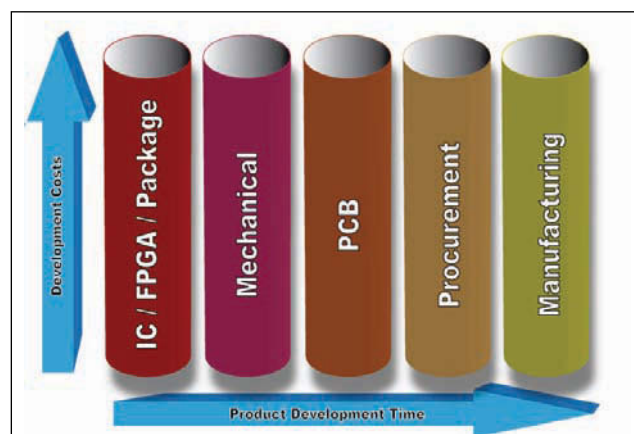


**FIGURE 1.** Spectrum analyzer board with mixed analog, digital, and RF circuitry. Courtesy of Agilent Technologies.

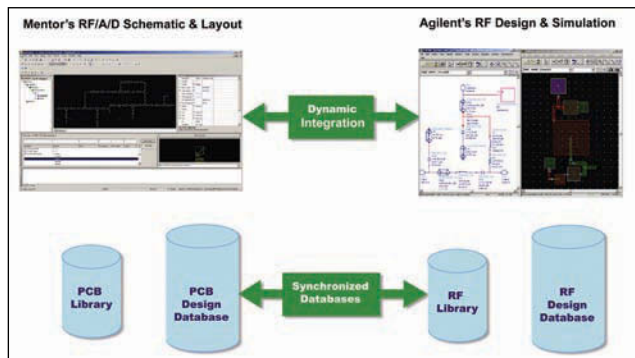
iPhone, where just months after the first introduction, the price of a unit was reduced by hundreds of dollars and Apple's inability to ramp production to full volume in the first months cost millions in profit. Even in the non-consumer automotive industries, time-to-market is becoming an important business requirement and driver.

The second common need and driver in today's competitive world is reduced development costs. Making designers more productive and adding efficiencies to the total product development process all affect the bottom line and enables companies to produce more profitable products with their limited resources. Removing wasted efforts and enabling designers to focus on the product — not how to use design tools — gives them more time to innovate, which leads to the third business need.

That third need is to produce more competitive products (more functionality in smaller spaces at lower product cost).



**FIGURE 2.** "Silos" in the standard product development process.

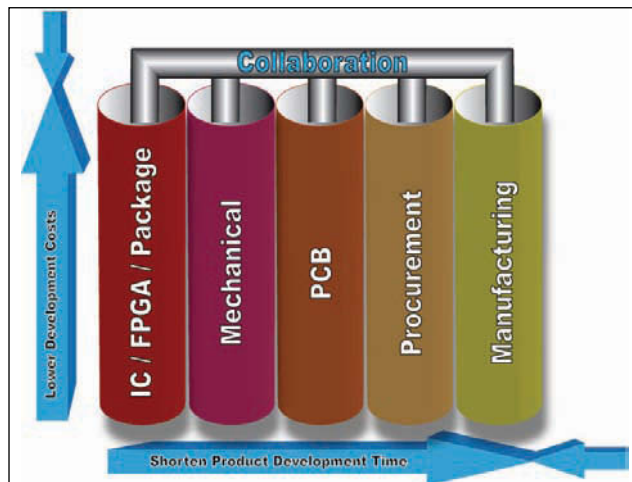


**FIGURE 3.** Integrating RF with the rest of the PCB design can reduce cycle times and produce a more competitive product.

Unfortunately, this is often at odds with the first two business requirements. More competitive products often require the use of advanced IC, FPGA, and PCB fabrication technologies, which adds to the complexity of the design process.

### Industry Trends Increase Design Complexity

We have all heard the expression, “the world is going global,” and this really applies to the electronics industry. Not all that long ago, the design and manufacture of electronic products of any significant complexity were performed in the U.S. or Europe. In recent years, China ramped up its manufacturing capabilities so that it can now produce equally sophisticated products. Companies in the U.S. and



**FIGURE 4.** Only sophisticated design flows can provide what is necessary to meet electronics companies' business needs.

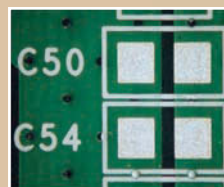
Europe now routinely outsource much of their manufacturing to facilities overseas. Following the manufacturing, design talent in countries like China is also rapidly improving and many companies are outsourcing all or part of their designs as well. So “going global” means that not only must companies compete with countries like China, but also leverage the talent in China while protecting internal IP, managing an increasingly complex infrastructure, and creating differentiated products.

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Creating differentiated products often requires the use of the most advanced technologies. IC and FPGA offerings continue to advance following Moore's law. Data transfer rates in the multi-gigabit per second range and pin counts in the thousands per package create PCB design problems. Implementing these high-speed, high-density components requires the use of advanced PCB fabrication technologies like HDI and microvias, and embedded passives in order to fit and route all the components onto the PCB. Meeting interconnect delay signal integrity constraints adds to the complexity, as many designs now have 50 to 80% high-speed nets.

Another trend we see rapidly emerging in many industries is the use of RF circuitry incorporated into an analog and digital board. Long present in the military and aerospace industry, this technology is now prevalent in wireless telecom, automotive, medical, industrial, and consumer goods. These system designs may contain several sections of RF that are tightly packed into sections of an analog or digital board, as illustrated in **FIGURE 1**.

### PCB Design – The Center of the Universe?

Most PCB designers tend to focus solely on the PCB design problems and processes, but product design requires much more than the PCB. To meet our companies' business needs we must consider productivity and process efficiencies in the complete product development process. In many compa-

nies, organizational boundaries and lack of communication capabilities between the various disciplines creates "silos" (**FIGURE 2**) that tend to isolate potential teams and create development process inefficiencies.

A company's aggressive business needs requires product developers to meet not only higher productivity goals within all of the design and manufacturing disciplines, but also improve efficiency *between* all of the design and manufacturing disciplines. This in the face of increasing complexities in the product designs itself, and the fact that these various organizations may be spread around the country or even the world.

Some of the burden falls to EDA suppliers like Mentor Graphics who must not only provide *incremental* improvements in their functionality, but also supply innovative new technologies that enable *quantum leaps* in productivity and process efficiency. Some of these "leaps" must extend outside of the PCB design domain and form bridges (or a collaborations) between PCB design and the other disciplines in the development process.

**Collaboration – Intellectual Property Management and Access.** A company's intellectual property (IP) comes in many forms including component libraries, reusable design data, design-in-progress data, constraints (high speed and manufacturing) and design intent, design and manufacturing best practices, preferred tool flows, etc. IP is of little use unless it can be managed and made available to all members of the design team on a timely basis. Electronic CAD (ECAD) data management systems integrated with PLM and ERP systems must provide the necessary management of and access to the IP.

**Collaboration – Between ECAD Disciplines.** Most competitive designs contain one or more high-speed, high-density ICs or FPGAs. As previously noted, an increasing number of designs now contain a mixture of RF incorporated into analog and digital sections of a PCB. Providing the ability for these various disciplines to collaborate on a product design can significantly improve the productivity of the individual designers, and also produce a more competitive product. For example, being able to assign the I/O pins on an FPGA in the context of the PCB (versus independently without consideration for PCB interconnect) can significantly reduce routing lengths, improve performance, reduce PCB designer routing time, and can even reduce PCB cost by reducing the number of board layers.

In the past, RF design was performed independently of the PCB design. Recently, RF design and simulation specialty products have been closely integrated with analog and digital design systems to create a collaborative team environment, as shown in **FIGURE 3**.

**Collaboration – Beyond ECAD.** Extending collaboration into other disciplines beyond electronic design can also make a big difference in process efficiency. An example is to create a collaborative environment where the ECAD and MCAD designers communicate during the design process electronically rather than using paper. The typical method of paper communication to proposed changes, either from the ECAD engineer or the MCAD



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designer, is a long, cumbersome, and error prone process. By implementing collaboration tools, when a change is proposed, the change can be communicated to the other disciplines who have the opportunity to view the proposal in a familiar environment (viewed in a typical PCB layout tool or mechanical 3-D tool respectively), comment, offer a counter proposal or approve the change, and then have that communicated back to the proposing party. All of this, in real time, represents a significant improvement over paper communication methods.

Collaboration between ECAD and the rest of the enterprise *throughout* the design process can also significantly affect the product development process efficiency, and may even mean the difference between a profitable and non-profitable product. Prime examples include real-time collaboration between ECAD, manufacturing and procurement. For example, electronically communicating a proposed PCB design change (a different component) to procurement and manufacturing give them the opportunity to review the proposal for volume purchase, price, and manufacturability in real time. This is especially important when design and manufacturing may take place at different locations around the world.

### The Cost of Being Competitive

All of the trends and technology discussed lead to one conclusion: ECAD systems that provide this level of design capa-

bilities are highly sophisticated. They are tightly integrated flows with IP management and integrated into corporate systems. They contain design capabilities for the most advanced technologies with easy-to-use human interfaces. They extend beyond PCB design and provide collaboration with other disciplines within ECAD, and on to other product development and manufacturing organizations. Collaboration connects the silos together, as illustrated in **FIGURE 4**.

These sophisticated design flows require extensive R&D investment to develop, deliver to users, and support. These systems do not come cheap, but electronic companies are switching from commodity PCB design systems to ones that can provide this level of product development support are realizing that investing in these systems puts them at a competitive advantage. Companies are also investing in the infrastructure support and training required to operate these systems. We even see countries like China that previously survived on low-end design systems now switching to systems containing the most innovative technologies available. Be cautious, U.S., Japan and Europe! Competition will only get tougher. **PCD&F**

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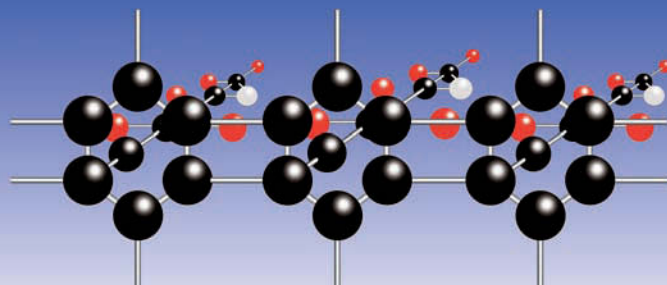
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热管理对LED的性能起着关键性的作用，因为寿命是结温的函数。LED系统制造商针对这个挑战，寻求改进的散热器设计、高效率的电路板、高热导率的附件和其它先进的热设计技术。LED为需要系统级协作设计提供理想的模型。当热考虑对推动性能那么重要，每一元件需小心计入成功的产品设计。要达成这些目标，热仿真真正扮演着一个越来越重要的角色，能够评估不同的选择，并在原型阶段前从热的角度优化系统级设计。最新嵌入CAD的热与流体仿真软件让设计工程师可诊断热的问题，评估其它设计，并快速重复至最优化的解决方案。

# SOLVING SYSTEM LEVEL Thermal Management Challenges

Thermal management is critical to overall system performance so mechanical designers need to consider thermal issues from the earliest stages of the design. by DR. JOHN PARRY

The United States Department of Energy (DoE) heralds LED lighting technology because it offers significant energy saving opportunities while enhancing the quality of the building environment. Thermal management is critical to LED performance because the useful service life of the LED is a function of junction temperature. LED system manufacturers are addressing this challenge by seeking out improved heatsink designs, high efficiency circuit boards, high thermal conductivity enclosures and other advanced thermal design techniques. The LED offers an ideal model of the need for system level co-design. When thermal considerations are so overwhelming a performance driver, every component needs to be carefully factored into a successful product design. To meet these objectives, thermal simulation is playing an increasingly important role because of its capability to evaluate alternatives and optimize the system-level design from a thermal standpoint prior to the prototype phase.

## Emergence of LED lighting

Solid-state lighting is a pivotal emerging technology that promises to fundamentally alter lighting options in the future. LEDs were originally designed to operate with less than 50 milliwatts of electric power. Over the last decade, LED power consumption has decreased dramatically, to 40 to 80 lm/watt. Besides energy efficiency, LEDs also offer longer life, and depending on the manufacturer and type, the useful life for white LEDs can range from approximately 6,000 hours to more than 50,000 hours. This compares to 30,000 hours for fluorescent tubes and less than 2,000 hours for incandescent bulbs. LEDs can also be manufactured to emit light of a specific color without the use of filters.

Market analysis firm Yole Développement says that high power LEDs will drive growth in the solid state lighting market, starting at well under \$1 billion in revenue in 2007

to approximately \$10.3 billion in 2012. Yole projects that high-brightness and ultrahigh-brightness LEDs sales will be responsible for about \$4.45 billion of that total, over 5.5 times the \$783 million market size in 2007. "These solid state lighting devices are rapidly becoming the lighting source of choice for diverse applications that include traffic signals, interior and exterior lighting in cars and trucks, large screen visual displays, and small LCD backlighting and decorative illumination," a recent iSuppli report states<sup>1</sup>. "And new lighting applications are constantly being discovered."

## Thermal challenges

High-powered LEDs provide greater thermal challenges than most other light sources, largely because LEDs don't generate infrared radiation. According to the U.S. Department of Energy, 75% to 85% of energy used to drive LEDs is converted to heat "... and must be conducted from the LED die to the underlying circuit board and heatsink, housings or luminaire frame elements." The US DoE's Office of Energy Efficiency & Renewable Energy has produced a fact sheet on "Thermal Management of White LEDs<sup>2</sup>". In the short term, excess heat can reduce an LED's light output and produces a color shift. However, another reason thermal management is so important is the long-term effects that include accelerated reduction in light output resulting in a shortened useful life. The DoE says that manufacturers normally test LEDs at a fixed junction temperature of 25°C. On the other hand, under constant operation the junction temperature is typically 60°C or greater and under these conditions the LEDs light output may be 10% or more below the rating, and could be significantly higher for products with inadequate thermal design.

For tungsten light bulbs, the heat flow path moves

directly from the filament to its surroundings by thermal radiation with some conduction due to the glass. The primary path of heat transfer in an LED device is usually from the junction to the system enclosure. The LED device manufacturer provides the package level thermal management. For the manufacturer, the biggest concern is minimizing the thermal resistance from the junction to the outside of the package. Some LEDs, typically small devices mounted on panels, have leads that form the main thermal conduction path and for these devices the thermal resistance from the junction to the leads is most critical.

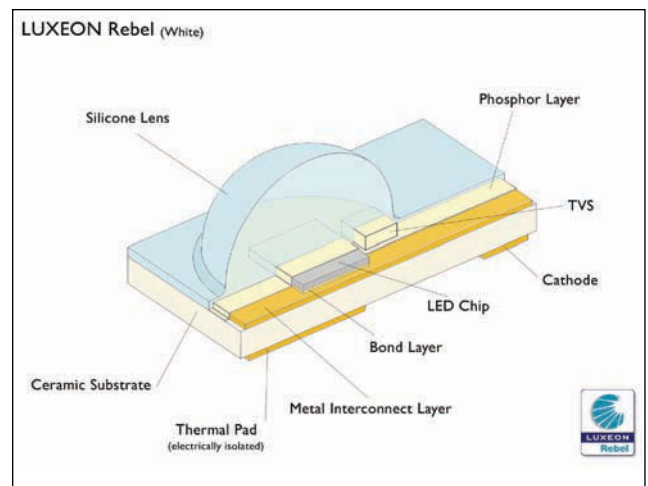
Package design varies by manufacturer and type of LED, but the concepts between packages are similar. In **FIGURE 1**, the LED chip is typically attached by a bond layer to a metal interconnect layer which is then attached to a ceramic substrate and an electrically isolated thermal pad. The entire package is designed to maximize optical output and move heat away from the back of the LED chip.

Rudi Hechfellner, applications manager for Philips Lumileds Lighting, San Jose, California says that thermal management is by far the most critical aspect of LED system design. Hechfellner pointed out that even the most thermally efficient LED devices requires that a cooling system be developed around it. He said that because most traditional lighting methods radiate heat, they do not have that level of thermal issues. Many systems manufacturers have much more experience in the electrical and mechanical than in the thermal aspects of design. “What the engineering community needs is a change of their mindset and think thermal first and electrical later,” Hechfellner said. “Thermal represents 90% of today’s design challenges for LED systems manufacturers while electrical and mechanical together provide only 10%.”

The nature of an LED package is such that even as LEDs increase in efficiency, the challenge of thermal management will not disappear. As light output reduces with temperature, a greater proportion of the electrical power is turned into heat, further increasing the temperature. The light output from an LED reduces as it ages, so its heat output may increase over time, accelerating the rate of degradation. A common cause of lumen depreciation in white LEDs is a yellowing of the phosphor, which may be heat or environmentally induced but does not necessarily mean that the chip is working less efficiently or that there is more heat being generated. Thermal management solutions must become more effective in removing the heat dissipated by an LED over its useful life.

### System Level Design Considerations

The design considerations are different for every LED and care must be taken to understand the metrics and performance of the LED being used in the application. The essence of LED system design is transferring the heat efficiently from the LED thermal spreader, slug or wire leads to the ambient surroundings. First of all, a secure and thermally efficient bond must be provided between the slug and the circuit board pad. The thermal connection typically runs through a small thermal via in the PCB to a large copper area on



**FIGURE 1.** Schematic of a high-power LED package.

another layer. Heat is typically conducted through this layer to the enclosure or an external heatsink. Understanding these system level thermal management challenges are integral right from the start, in the PCB design phase.

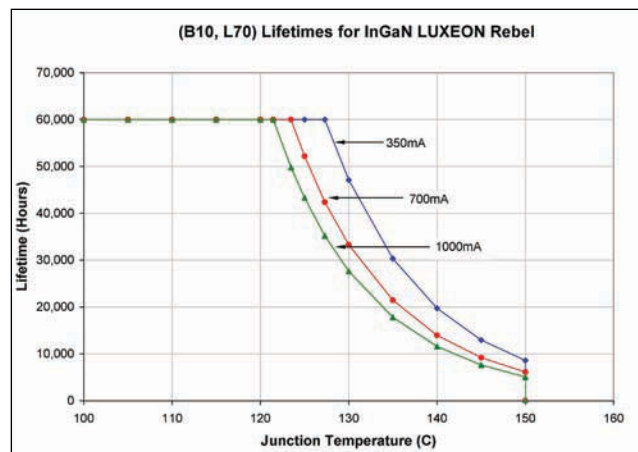
An external heatsink may be required in situations where an exceptionally large amount of heat is dissipated within the enclosure. Copper and aluminum are commonly used materials for LED heat sinks. Optimizing the geometry of the heat sink is a critical concern in many applications, as the heatsink-to-air thermal resistance is often significant. Heat sink performance varies depending upon factors such as the material, number of fins, fin thickness, base thickness, etc. External heatsinks extend the surface area available for heat to transfer to the ambient air. The optimum design depends on the local air flow conditions that are affected by the introduction of the heatsink, increasing the design challenge.

Copper offers superior thermal conductivity, while aluminum is lighter and less expensive. In some cases, PCBs made of materials that improve heat transfer through the board may be used. These boards may be made of ceramic, coated steel, aluminum or some of the newer, thermally enhanced PCB laminate materials.

The most difficult LED applications are those that require an airtight enclosure to protect the LED from its environment. One way to address this challenge is to use an enclosure material having a high thermal conductivity. In other cases, more elaborate measures may be required. One example is an air-to-air heat exchanger design that uses internal fans to circulate hot air over internal fins, which conducts the heat into the walls of the enclosure. External fans are then used to move cool ambient air over fins fitted to the outside of the enclosure and remove the heat. Heat transfer is then via a series of convection and conduction steps.

Obviously, there are a large number of design variables that need to be considered when designing LED systems. Optimizing the thermal design is critical for a number of reasons. The DoE’s fact sheet on thermal management notes that excess heat affects both short-term and long-term LED performance. The reversible short-term effects are color shift and reduced light output. Minimizing color shift is critical for back lighting





**FIGURE 2.** Expected lifetimes for InGaN LUXEON Rebel at various junction temperatures and drive currents at a 90 confidence level.

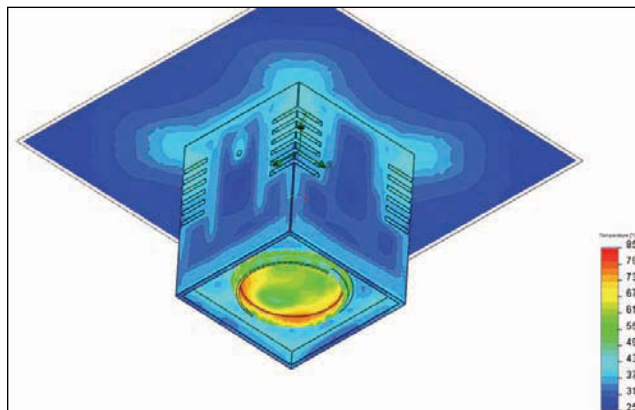
in emerging applications such as LCD TVs where increasing the LED density improves the color variation in the image but makes the cooling more challenging.

Increased junction temperature can severely affect lifetime and reliability performance of a power LED. For example, all other things being equal, a 10 degree change in junction temperature has a dramatic effect on lifetime and reliability as shown in **FIGURE 2**. Optimizing the thermal design may also have a major impact on product cost. For example, the effectiveness of the thermal design may determine whether or not it is necessary to use a heatsink, a decision that will substantially affect the overall cost. System co-design that brings the PCB into the thermal equation early in the design process can help off-set these costs by integrating novel cooling solutions at the circuit board level.

### Role of Simulation

Most electronics and original equipment manufacturers (OEMs) and component suppliers have long accepted the need to identify and resolve thermal issues early in the design process. Many have adopted software that performs component- and system-level analysis to address thermal management prior to physical testing, with the goal of avoiding additional design iterations. However, manufacturers of LED systems frequently design systems built around other lighting technologies that do not provide the same thermal management challenges. These companies may not have the required knowledge and expertise to use the powerful and sophisticated computational fluid dynamics (CFD) software used by semiconductor device manufacturers, printed circuit board designers and large electronics OEMs.

The CFD codes of a decade ago and even many used today require the user to have a deep understanding of the computational aspects of fluid dynamics in order to obtain accurate results. For example, users need to know how to translate their computer aided design model into the CFD environment, then “reverse” the model so that empty flow space (rather than the solid product) is modeled, to create an overall mesh with the right properties, determine boundary conditions, select the right physical



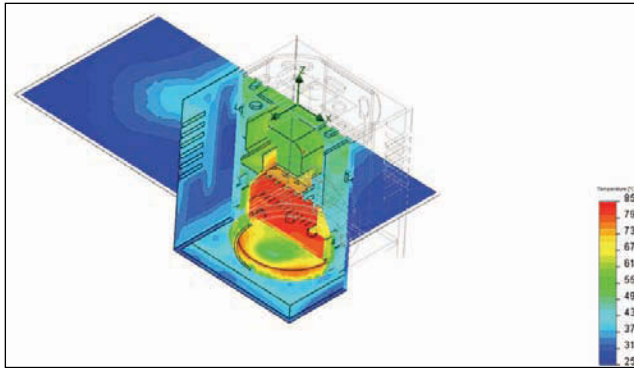
**FIGURE 3.** Surface temperatures of the entire lamp.

models, tweak solver settings to ensure convergence, as well as other tasks. Previous generations of CFD software also required a substantial amount of tuning and tweaking, such as manually modifying cells to improve the mesh quality or adjusting solver controls, or relaxation factors, in an effort to get the software to converge to a solution.

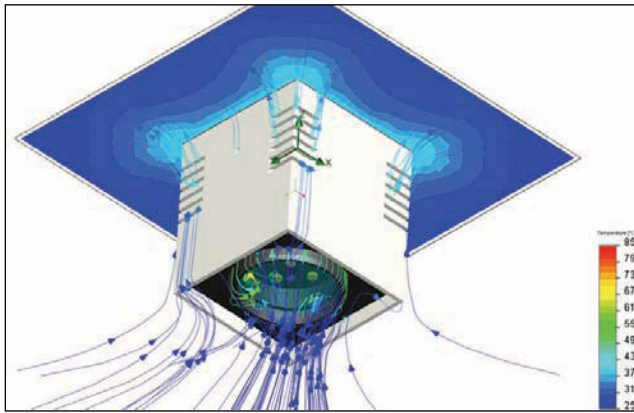
But in the last few years a new generation of CFD software has been introduced that addresses the major reasons for its relative lack of use. The new software uses native 3-D CAD data, automatic detection and gridding of the flow space, and manages flow parameters as object-based features, eliminating the need for engineers to understand the computational part of CFD, allowing them to focus on the fluid dynamics of the product that is their responsibility to understand and master. The newest generation of CFD software contains sophisticated automatic control functions that ensure convergence in almost every application without the need for manual tuning.

This new generation of software is well suited to the thermal design of LED systems. The skills required to operate the CFD software are simply a knowledge of the CAD system and the physics of the product, both of which the vast majority of design engineers already possess. The ability to utilize the native 3-D CAD saves time and makes it possible to capture the full geometric complexity of LED systems. The new generation of software also covers all of the possible thermal transfer mechanisms so it can be relied upon for accurate analysis. By automating the steps required in creating a CFD model, the new generation of CFD software makes it possible for LED systems designers to evaluate a large number of design alternatives very quickly.

The lamp shown in **FIGURES 3, 4 and 5** uses six high power LEDs with a built-in power supply that dissipates heat. Since no fans were used, design engineers could only count on conduction, natural convection and radiation to remove the heat. Using a CFD software package embedded in their CAD system, Voxdale engineers defined all the materials and their characteristics, the heat dissipation for LEDs and power supply, gravity direction for convection, etc. After automatic meshing and solving, the results were visualized on the native CAD geometry as shown in the figures.



**FIGURE 4.** Temperatures inside the lamp shown with a 50% slice.



**FIGURE 5.** Visualization of the flow trajectories (through convection). Convection brings cold air inside the lamp while hot air escapes through the slots.

### Physical Testing

Physical testing is too costly and time consuming an approach to use to investigate speculative design changes, but is highly effective for both validating the final design and in investigating manufacturing issues. Physical testing can confirm the material property values used in the simulation check bond line thickness, and identify problems such as voids in the die attach.

The leading approach takes advantage of the fact that the temperature is proportional to the forward voltage drop of a specific device. After determining the forward voltage drop at a specific measurement current, a large current is applied to heat the LED. Then this current is turned off while another much smaller test current is applied to make the measurement. The test current used to characterize the device and the forward voltage have to be identical. The forward voltage is measured very quickly before the junction has the chance to cool down. The ability to monitor the temperature change with respect to time can provide detailed information on how heat flows through each layer in the path from the junction outwards. This allows direct measurement of the key thermal resistances in the heat flow path, such as the die attach resistance.

Sophisticated measurement hardware that can measure the temperature change of the device within a few microseconds of being powered off is required, due to the LED's fast thermal response. This type of thermal transient measurements can be used to generate highly accurate "struc-

ture functions" which provide detailed internal information for power-LED packages, revealing die-attach failures and other structural integrity problems.

### Conclusions

LED technology offers enormous potential to save energy and enhance lighting quality and reliability. Thermal management is critical in LED design in order to meet performance, service life and cost requirements. Systems designers have a wide range of options to consider in meeting thermal challenges. The latest generation of CAD-embedded thermal and fluid simulation software enables design engineers to diagnose thermal problems, evaluate alternative designs, and iterate rapidly to an optimal solution. The final design can be qualified with measurements at the prototyping stage to ensure manufactured tolerances (e.g., interface thicknesses) meet the thermal design requirements and to identify any manufacturing problems. The knowledge gained can be used to improve future design simulations. [PCD&F](#)

### REFERENCES

1. Rebello, Jagdish, iSuppli – "The Solid State Lighting Industry: At a Critical Crossroad," September, 2006.
2. U.S. Department of Energy, Energy Efficiency and Renewable Energy, Bulletin PNNL-SA-51901, "Thermal Management of White LEDs," February 2007.
3. Philips White Paper, "Understanding Power LED Lifetime Analysis."

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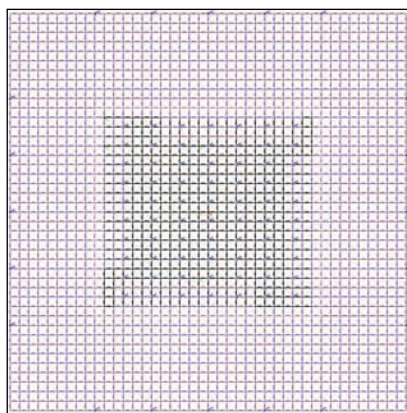
# Innovative Modeling Supports CO-DESIGN of the POWER SUPPLY CHAIN, Part 1

New software tools ease problems associated with power delivery design in large computer systems. by DAVID QUINT and CHARLES KEEN

In the late 1990s, the Hewlett-Packard Company entered the marketplace with a large server under the name “Superdome.” This event actually represented a new dimension in the integrated circuit and package design area. The voltage/current pinch and clocking frequencies of the IC’s contained in this new system had increased so dramatically that designers had to design a new tool to model and simulate the power delivery system (PDS) with a higher level of detail.

A voltage/current “pinch” had occurred when designers used lower voltages and higher currents at the integrated circuit level in order to pack more gates in the same amount of silicon area without increasing power density. This new generation of IC technology allowed increased complexity while maintaining power per unit area. However, it also created this “pinch” for power delivery, since current increases drawn by the IC, are inverse to the supply voltage, and create larger  $I \cdot R$  and  $L \cdot dI/dt$  drops in the package, the PCB, and the converter. The “pinch” was tightened by smaller voltage tolerances scaled to the lower supply voltages. Higher currents stress package power planes, solder joints, and PCB power planes, causing excessive heating and reliability problems.

Since that time, there has been the opportunity to redesign several CPU and ASIC packages and learn a great deal in the process. These techniques include a suite of simulations that evaluate the performance of the integrated system from several viewpoints, including methods of interfacing between the IC, the package, and the printed circuit board, either using a fully detailed package model, or with a simplified (IBIS-like) model. The use of simplified models for assemblies, including the packaged IC, can be a time saver, especially if the simplified model is used multiple times at the next level of simulation.



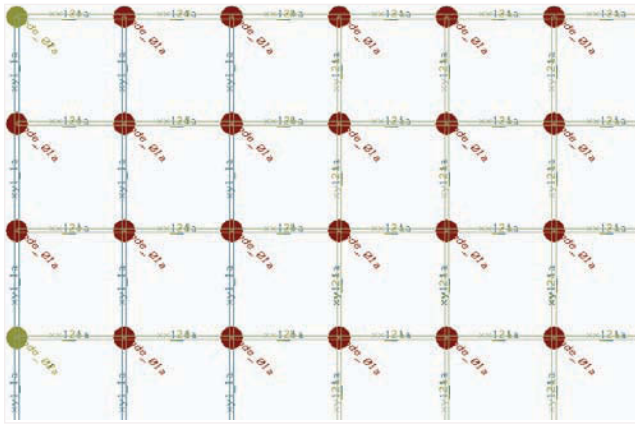
**FIGURE 1.** Graphical depiction of the SPICE model of a package, two layers superimposed, to illustrate the level of detail of the model.

The original tool was actually a large scale SPICE model built in three dimensions. Planar constructions such as IC packages and printed circuit boards can be represented by a stack of two-dimensional square grids, representing the conducting planes, connected vertically with simple circuits representing vias or groups of vias, as shown in **FIGURE 1**. Planes and vias are represented as sub circuits including inductances, inter-plane capacitance and resistors as lossy components. Components such as capacitors and resistors are represented with sub circuits, including parasitics of the components and connecting vias.

The IC can be represented by a grid of time varying resistors, bypass capacitors, and parasitics, rather like a multi-port IBIS model. The graphical depiction used by the tool is not a conventional schematic, but a map of lines and circles with labels. The model is assembled with the use of a script, which leaves a two-and-one-half dimensional depiction that can be edited manually.

The final graphical model shown in **FIGURE 2** is then processed into a three-dimensional SPICE deck, which is a massive interconnection of sub circuits. The components of the sub circuits must then be evaluated by the user, which is





**FIGURE 2.** Above figure zoomed in to show the individual bars, circles, and notes that identify the sub-circuits, each of which contains one R, one L, and one C.

not as daunting a task as it may seem. This SPICE circuit can then be evaluated, yielding voltages, currents, powers, etc. at almost any location within the package. The model is ready for SPICE evaluation in any mode: DC, AC, and Transient simulations can all be done on the same model with minor modifications.

Since the graphical interface does not depend on extraction from a layout tool, it is easily modified for speculative changes and can be used at an early stage in the system design process. On the other hand, most power analysis tools do their models from an extraction of design layout information of an EDA tool. This appears to be a convenience for the power designer, but it delays critical design decisions until late in the design process. We have found that, even though the accuracy of the layout may be less than ideal, the ability to evaluate the performance at an early stage is highly desirable.

A common problem with all PDS analysis tools appears to be the complexity of doing the analysis itself. The device being modeled must be divided into a large number of sub-sections in order to accurately capture the geometric effects of small features. For example, we have found that CPU run times of a week or more can easily happen where a large package is concerned. Where long run time is necessary with a system model, computation time can be speeded up considerably by partitioning the model and substituting simplified units for certain sections of the system model. The simplified model can also enhance communication between levels of the system where the IC design, package design, and system board design are done by different groups. The final section of this paper seeks to explain some of these techniques.

Until recently, the SPICE model approach to package and board analysis was running out of steam because run times were getting too long. In the course of trying to speed up SPICE simulations, we tried comparing different vendors' SPICE products using the same circuit. We determined that the compute time for at least one new SPICE engine was dramatically improved. For example, we found that a 25,000 node SPICE model could be run in about 20 minutes using a newer SPICE solver where it had taken more than eight days previously. This decrease in processing time is a significant productivity factor.

## Power Delivery System Evaluations

The first simulations with the three-dimensional models yielded much more information, and more accurately, than we had ever created before. Much of this accuracy came from the use of a distributed model. With that information in hand, engineers quickly embraced the process, using the new data mainly to improve design accuracy and reduce project risks. Prior to this, the power delivery modeling consisted of a manually calculated one-dimensional network, with consequent errors that often required late corrections based on measurements.

A new process for evaluation of the PDS evolved to include six distinct categories of performance metrics. The important point is that not all of the information produced by the new analysis is useful, so there must be a system for evaluating the data. Some of these categories are more important than others, and my purpose is to explain the importance of each one. Briefly, the six categories are:

**DC Voltage Drop.** This can be done with a uniform current or detailed map of currents across the die. Actual currents in full activity are used here. The results can determine if excessive voltage drops occur at specific locations on the die. In addition, currents measured at the C4 or bump locations can reveal current density issues or locations exceeding current specifications. In the PC board context, excessive voltage drops and localized heating of planes and vias are

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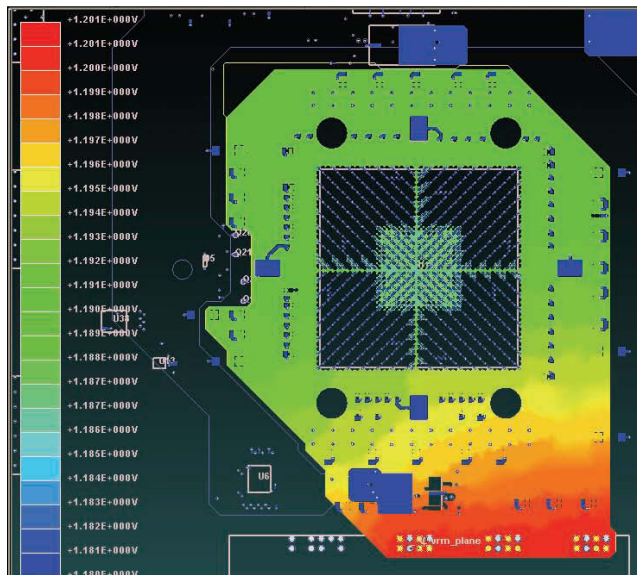
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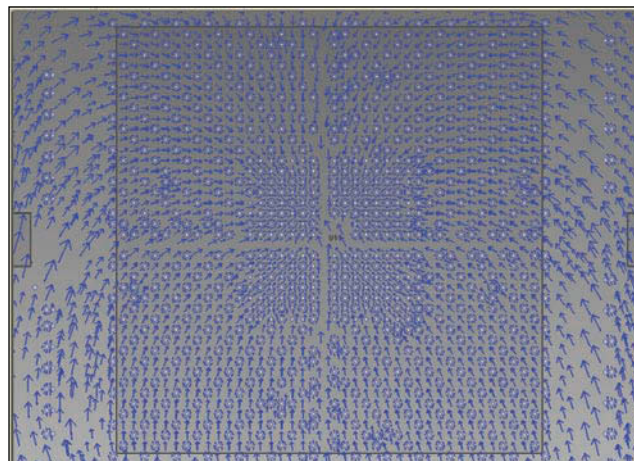
**FIGURE 3.** Voltage map in a 1.2V power plane with a large ASIC near center. VRM source is toward the bottom. Voltage contours can be seen in gray scale, where the original is in color. Plots of this type can highlight hot spots and/or suggest layout improvements to improve performance.

important issues. The information can also be used to locate sense points for voltage regulation.

**AC Impedance looking into the PDS.** From the IC perspective, the package PDS has an equivalent impedance vs. frequency. IC parasitics and bypass need to be included to simulate the response of the merged system. The IC model is a grid of current sources, which add up to 1 amp, all phases at zero. These sweeps can be useful primarily to observe those components or features causing PDS resonances. Beyond that, the model can be used to optimize the frequency response of the PDS by damping out or moving resonances to provide a flatter  $Z(f)$ . This is easily done by trial and error, by changing bypass cap values and locations. The results of this action can be seen graphically in the transient simulations shown. The die circuit will usually be divided into several blocks, with different current loads, so the single impedance value may not be precise enough for a large IC, and the distributed model would be required. In addition, there may be several power domains that would need to be evaluated individually.

**Transient Step Current.** This test requires some knowledge of the steady-state operating points of the IC, including leakage and active currents. Generally, the die will be at a low current state if it is idle from a processing standpoint, and jump to a high current draw when called up to full activity. This will produce a “dip” in voltage followed by an overshoot and ringing. This is the most fundamental characteristic of the IC current, and it can reveal problems with inadequate die, package bypassing or PDS resonances. Determining the level of activity or the rise time of the current steps on other vendor’s parts can be difficult to obtain.

**Killer Virus Time Domain Simulation.** This is an extension of the transient step current simulation. It is possible,



**FIGURE 4.** Current map of the board PDS plane underneath the ASIC. The current magnitudes in the actual plot are color coded. Plots of this type can highlight current pinches and hot spots.

though not likely, that the operation of the die could be directed to cycle from high to low and back at a frequency corresponding to a resonance of the PDS. In this case, the die cyclical voltage could increase in amplitude over several cycles and kill the operation of the die. In simulation testing, this is still considered to be the worst possible stress of the PDS.

**Transient Active Current.** Once the die design has progressed enough to determine the high frequency switching current drawn by the circuit blocks, these currents can be simulated in the PDS model. The IBIS-like load models are driven separately, or in blocks to fill the grid of die connections. This could also be done in AC mode, but IC designers generally find the time domain graphs more useful. For example, transient current events on the die can occur at the clock frequency, which is usually many hundreds of megahertz and may cause the supply voltage to drop below spec. These transients are usually well above the useful frequency range of the package bypass design. Faced with this, the IC designers can take actions to move timing events to reduce current spikes, or increase die bypass capacitance. Also, this simulation yields a great deal of information at the package/PC board interface which can be used to generate specifications and/or simplified models for PC board designers.

**Leakage of High Frequency Noise.** When generated at the die level into the PC board power domain, this is a difficult problem to simulate. This could contribute to EMI problems and/or create power related interactions that could limit performance, especially where a large number of IC’s are used in close proximity. Usually, the same model for the package can be used, but the simulation needs to be modified slightly to measure the effects in question.

## DC Voltage Drop

This is the most fundamental criterion for the operation of the circuitry on a system board. As simple as it may seem, it should not be taken lightly. The problem can be as simple or as complex as the package or board layout. The voltage/current pinch can happen at any point in the system, and



if the designer does not have a good two- or three-dimensional simulation capability, significant errors or omissions can be hidden from view. Voltages in the printed circuit board can usually be probed to find excessive drops. This information is particularly useful in determining the proper copper thickness to use for the power and ground planes, or if additional planes are needed in the board stack up. Currents can be measured in planes and vias to look for places where overheating may occur. This can be a serious problem, particularly under parts with very small pitch and high current densities. In the past, most boards were designed without 2-D simulations. However, the changing industry is putting a "pinch" on costs and time to market as well, so the lab that has the better tool set for board design will have the advantage of fewer board turnarounds.

Errors in the package are much harder to fix, since prototype turnaround times are much longer for packages, and costs are higher. The package designer must have accurate knowledge of the DC current drawn by the IC, including the distribution map for a larger die. A three-dimensional model of the package power circuit may be essential to finding overheated bonds or vias and localized voltage drops as well as heating of the planes of the package.

**FIGURE 3** illustrates a plot of supply voltages on a certain power plane within a PC board. The actual plot is in color, which allows voltage drop are subject to be more easily seen. There are no problems in this design, but it illustrates that the current distribution and voltage drop is subject to the shapes of the planes, the placement of sources and loads, and even upon the presence of via keep-outs and thermal relief patterns, which all increase the effective resistance of the planes. Currents can also be displayed as in **FIGURE 4**, and hot spots and current pinch areas can usually be found. Computer displays will take advantage of colors to display magnitudes.

There are a number of problems associated with delivering power reliably within a large computer system. Many smaller system manufacturers have not had to deal with these issues on a large scale, but advances in the technology are likely to make these problems much more commonplace. While there are many new software tools designed to deal with these technical hurdles, there is still some confusion surrounding how they are to be used, and how to correlate simulation data through the system hierarchy. In Part 2 of this article, we will propose an approach, including basic, essential, and advanced methods of measuring performance of the PDS, explore methods for linking the simulations of differ-

ent levels of the PDS, while at the same time simplifying and expediting the task. **PCD&F**

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# 'Warm' Manufacturing HEATS UP

Nanotechnology poses an attractive solution for lower-temp soldering. by DR. ALAN RAE, DR. ANDREW SKIPOR and MARC CHASON

Higher reflow process temperatures are causing concern among electronics manufacturers. Product reliability can be diminished by the residual stresses in PCB assemblies that these higher temperatures cause. Higher temperatures also require tougher qualification requirements for components and sometimes a significant change in manufacturing processes.<sup>1</sup>

Low-temperature or room temperature assembly processes have the potential to improve field reliability, streamline manufacturing and reduce cost. As nano-structured and more sensitive components are introduced, some with biological components that have to interface with electronic detection systems, lower-temperature assembly processes will become a necessity.

“Warm manufacturing” is a term coined by the International Electronics Manufacturing Initiative (iNEMI) to describe processes that can be used to assemble electronic devices at temperatures lower than traditional solder reflow. The need for warm manufacturing stems from:

- Higher Pb-free solder reflow temperatures increased failure rates of existing components and devices.
- Increased thermal sensitivity of newer devices that contain nanoscale semiconductor structures, MEMS devices, proteins and other low-temperature organic materials.

Several novel nanotechnology applications have shown great promise as solutions for warm manufacturing. Encompassing many diverse disciplines that permit the manipulation of matter at the atomic level, nanotechnology enables radically new approaches to material property enhancement and synthesis. Nanomaterial solutions have the potential to augment and enhance traditional manufacturing processes, improve existing products, enable new product concepts, and disrupt industry. Although none of the technical solutions currently available is sufficiently developed to provide a universal, easily integrated process for lower temperature assembly, initial work has shown encouraging results. This

article discusses some of these applications.

**Nano-solder: melting point depression.** An example of how nanotechnology can be used to modify assembly process temperatures is the excellent work over the past several years on melting point depression. The phenomenon of melting point depression of nanoscale metal particles has been studied since the 1960s, when it was noticed that extremely thin evaporated particles of metal have a lower melting point than the bulk material.<sup>2</sup> Melting point reduction of tin evaporated particles was studied by Wronski<sup>2</sup>, and the studies by Buffat and Borel on gold nanoscale particles demonstrated well over 50% melting point depression, compared to the bulk melting point of gold. More recently, other researchers<sup>3,4,5,6</sup> have developed alternate experimental methods, such as nanocalorimetry, to measure the latent heat of fusion as a function of temperature. This new calorimetric technique has been developed where nano-Joules of heat can be measured. Based on these nanocalorimetry studies, a simple expression was developed to relate melting point to particle size.<sup>5</sup>

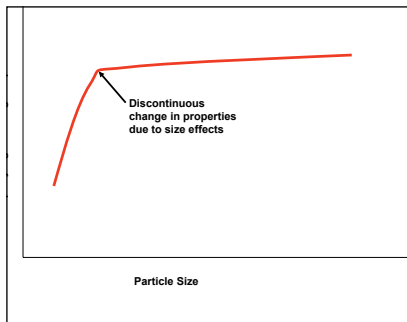
$$T_m(r) = 156.6 - (220/r) \quad (\text{EQ. 1})$$

where  $T_m(r)$  = melting temperature (°C).

$r$  = radius of the particle (nm).

This equation reveals that significant melting point suppression happens when the particle radius approaches the sub-20 nm range.

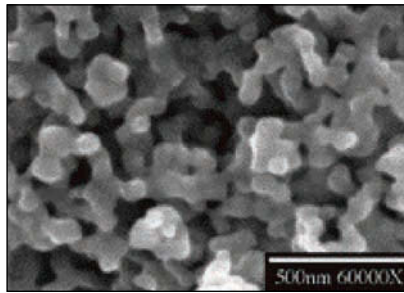
Many materials exhibit a change in properties as they move toward the nanoscale. This is because of the increase in the relative proportion of higher energy surface atoms. This change can be exhibited as a change in reactivity (e.g., sinterability or electromagnetic properties) driven by band gap changes that cause dramatic changes of electronic properties, or optical properties such as color and transparency. Where these changes occur – the tipping point – is a function of the individual element or compound and its environment,



**FIGURE 1.** The tipping point in properties found in many materials at the nanoscale.

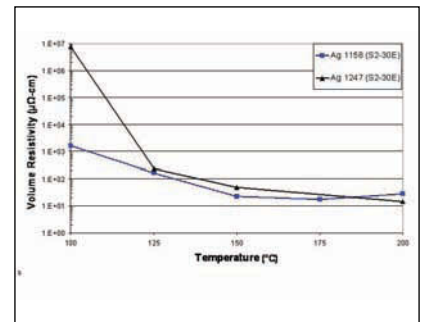
and normally occurs below 100 nm (**FIGURE 1**).

Solder materials containing nano-sized metals exploit the high surface area and high surface energy (think of it as stored energy) of nano-sized particles to lower the apparent melting point below the conventional melting point. Thus the melting points of tin, silver and copper, the ingredients of most popular Pb-free solders, all can be depressed below 200°C, well below the eutectic melting point of 217°C.<sup>7</sup>



**FIGURE 2.** Conductive network produced using heat-treated 80 nm silver.

Silver exhibits a dramatic increase in sinterability at temperatures below 200°C. Nano-silver powders can be produced in essentially monodisperse form using a “bottom-up” approach, in which nuclei grow under a protective polymer coat that permits metal atoms to accumulate, while acting as a charge director to keep the embryo crystals separated. The crystals are permitted to grow until the desired particle size is achieved; then the reaction is stopped and the crystals suspended in an appropriate vehicle or dried. The polymer



**FIGURE 3.** Resistivity as a function of process temperature for a 30 nm silver. Note the significant increase in conductivity as low as 125°C.

coating, which can be made hydrophilic or hydrophobic, aids re-dispersion and prevents spontaneous sintering of the dried silver particles. Pure nano-metals such as silver can be deposited by a range of printing techniques with a thermally removable binder. Even at 80 nm, significant densification and conductivity development is seen above 125°C (**FIGURES 2** and **3**). These show promise for die attach, conductor printing and electrical connections.

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**FIGURE 4.** Water drop on hydrophobic 80 nm silver coating.

The iNEMI Nano-Solder Project is working to put these materials into a printable solder paste. The project team is characterizing the metals and working to develop a proof of concept demonstration, using a model similar to the SnAgCu system developed for Pb-free solders ([inemi.org/cms/projects/ba/Pb-free\\_nano-solder.html](http://inemi.org/cms/projects/ba/Pb-free_nano-solder.html)).

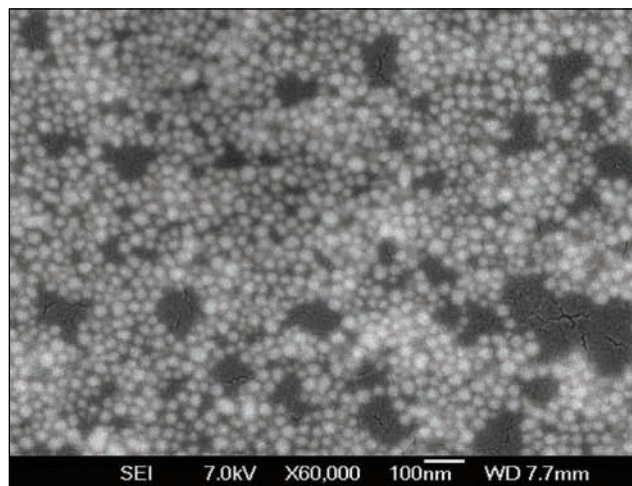
Nano-solders could potentially be available within the next three years. A method has been developed to synthesize lead-free solders such as Sn-3.5Ag-xCu ( $x=0.2, 0.5, 1.0$ ) by chemical reduction methods.<sup>8</sup> Sinterable silver systems are currently available from such companies as Cabot, Cima Nano-Tech and NanoDynamics.

**Enhanced adhesives.** Nanomaterials can enhance mechanical properties of adhesives (even a 0.1% addition of multi-wall carbon nanotubes can raise the flexural strength of an unfilled epoxy by 30%), as well as the electrical properties because of the large number of potential contact or tunneling events when nano-sized particles are present. A reduction of 10x in particle size (for example, from 1  $\mu\text{m}$  to 100 nm) with the same weight content yields a  $10 \times 10 \times 10$  (1000-fold) increase in the number of particles present.

Several iNEMI members are participating in a University of Binghamton SPIR project (Strategic Partnership for Industrial Resurgence, <http://watson.binghamton.edu/level2/industry.html#SPIR>) to quantify effects of nanoparticles – metal and carbon-based – in resin-based systems in order to get a consistent dataset to characterize performance. Information from this project will be published.

**Nano-attach technologies.** Hook-and-loop fasteners (e.g., Velcro) used the ideas generated by plant burrs to create a new fastening paradigm. An extension would be to use carbon nanotubes, as suggested by researchers at Michigan State University in 2003.<sup>9</sup> Simulation of entangled carbon nanotubes demonstrated nanotubes made in curved shapes could be used to develop very high-strength room temperature interconnects.

Another innovative application of nanotechnology is biomimetic nano-attach. Textured dry adhesives, based on the gecko foot approach (bio-inspired) where nano-sized hairs attach to surface roughness using van der Waals forces, have been the subject of a great deal of research.<sup>10,11</sup> Bio-inspired materials systems



**FIGURE 5.** Self-assembled silver nanoparticles monolayer on a polymer surface through hydrophobic surface modification of a normally hydrophilic system.

using carbon nanotubes or polymer nano-filaments have been demonstrated at a number of research locations with strengths far higher than those that comfortably attach a gecko to a ceiling!

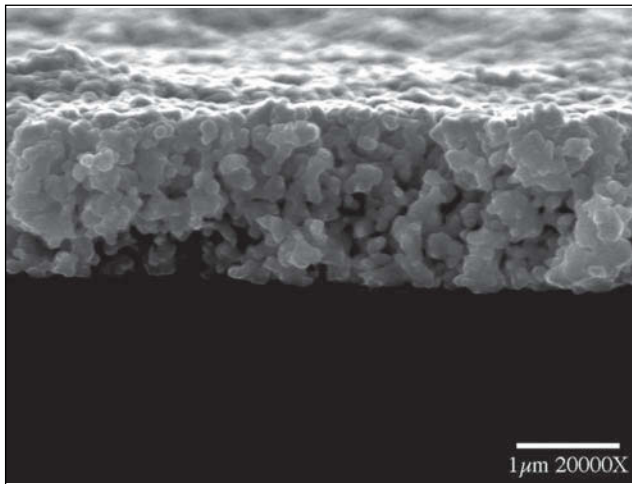
The iNEMI Nano-Attach research project is identifying and attempting to demonstrate these types of nano-adhesion techniques that have the potential to replace traditional solder or conductive adhesive assembly processes currently employed in electronics manufacturing.

## Implementation Challenges

**Percolation and particles.** The addition of fine particles to improve polymer system conductivity has been well documented in the literature. However, duplicating the performance in real-life systems tends to be much more complex. Nano-product implementation can only be achieved if the following factors are addressed:

- **Protective coating.** Virtually all nano-metals need a protective coating that permits dispersion in liquids and prevents oxidation or self-sintering. Uncoated silver will sinter to itself at room temperature, and uncoated copper will quickly turn black. Uncoated aluminum and many other metals are pyrophoric. Coatings may be applied in vapor phase by precipitation or chemical reaction.
- **Agglomeration.** Nanomaterials have high surface energy and tend to stick to each other. Because the number of particles per unit volume is high, the inter-particle distance is lowered as the particle size decreases for a given content. At the sub 5  $\mu\text{m}$  level, many colloids agglomerate at concentrations of only 3 to 5%.
- **Dispersion.** Nanoparticles supplied as dry powders are notoriously difficult to disperse in viscous liquids. The tendency now is to supply them as dispersions in compatible liquids or polymer master batches.
- **Segregation.** By varying the hydrophobic/hydrophilic nature of the surface coating, it is possible to encourage the material to disperse in a similar medium or to preferentially congregate on a second phase or at the surface (**FIGURES 4 and 5**).
- **Reactivity.** Reaction with catalysts, fillers or other





**FIGURE 6.** Printed 30 nm silver layer processed at 150°C.

constituents must be controlled; nanoparticles, by their nature, are reactive.

**Sinterable systems.** Many of the same issues of surface reactivity apply to sinterable systems (e.g., ink-jettable silver). Surface control is key to controlling reactivity, but the same compromises apply as in adhesives; particles have to be disagglomerated, remain in suspension and achieve a practical concentration and shelf life. The issue is compounded by the fact that many printing systems need relatively low viscosities (tens of centipoises – between the viscosity of water and milk) and many of the inorganic fillers to disperse have high specific gravity compared with the organic pigments we use in many applications. Silver, for instance, has a specific gravity of >11 (much greater than that of organic materials).

**Nano-solder.** One of the main issues in nano-solder production is the use of tin. It is a very reactive metal and readily oxidizes. (Most of the dross forming on SnPb solder is actually tin oxide.) It is, however, possible to produce tin particles in a reducing environment. Manufacturing oxide-free tin particles, integration of metal particles with flux, and electronics assembly are the focus of the iNEMI Nano-Solder Project. This work is enhanced by a project funded by the National Science Foundation at Purdue University and MetaMateria Partners that is exploring the mechanism of nano-solder consolidation.<sup>12</sup> The electron microscopy facility at the Purdue University Birck Nanotechnology Center is carrying out *in-situ* characterization of the melting behavior of tin and tin alloy nanoparticles. This analysis will be crucial for understanding the melting behavior of nanoparticles intended for use in a solder, and will allow the behavior of individual particles to be correlated with the behavior of a solder paste. This type of fundamental understanding of particle and paste behavior will be necessary for understanding and resolving the challenges related to developing a useable nano-solder.

**Nanotube “dry” adhesives.** Several challenges include producing the material in the correct form, verifying the theoretical strength and conductivity parameters, designing device interconnects and verifying processability and reliability – and doing it all economically. Nevertheless, this is a game-changing route to assembly that could have real benefits for electronics assemblers.

## Conclusion

Nanotechnology provides many useful tools to enhance the properties and processing of electronic materials. The enhanced materials and processes will have to prove their reliability and economic value to compete, but the sheer volume of opportunities and potential solutions suggests we’ll be seeing a lot more nanomaterials in our industry. **PCD&F**

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## REFERENCES

1. A. Rae and A. Skipor, “Nanotechnology and Room Temperature Assembly,” *SMTA: Emerging Technologies Summit*, Sept. 25, 2006.
2. C. R. M. Wronski, “The Size Dependence of the Melting Point of Small Particles of Tin,” *Brit J. Appl. Phys.*, vol. 18, 1967.
3. Ph. Buffat and J. P. Borel, “Size Effect on the Melting Temperature of Gold Particles,” *Physical Review A*, vol. 13, no. 6, June 1976.
4. S. L. Lai, J. Y. Guo, V. Petrova, G. Ramanath, L. H. Allen, “Size-Dependent Meeting Properties of Small Tin Particles: Nanocalorimetric Measurements,” *Physical Review Letters*, vol. 77, no. 1, July 1996.
5. Leslie H. Allen, “Nanocalorimetry Studies of Materials: Melting Point Depression and Magic Nanostructures,” *NNUN Abstracts 2002/Materials, Physics, Process & Characterization*, 2002, p. 40.
6. M. Zhang, et al, “Size Dependent Melting Point Depression of Nanostructures: Nanocalorimetric Measurements,” *Physical Review B*, vol. 62, no. 15, October 2000.
7. Kevin Grossklau, Melting and Coalescence Behavior of Tin Nanoparticles for Use in Low Temperature Solder Applications, Purdue University, master’s thesis, August 2007.
8. Lin-yin Hsiao and Jengong Duh, “Synthesis and Characterization of Lead free Solders with Sn-3.5Ag-xCu (x=0.2,0.5,1.0) Alloy Nanoparticles by the Chemical Reduction Method,” *J. of the Electrochemical Society*, 152, (9), 2005.
9. Savas Berber, Young-Kyun Kwon and David Tamanek, “Bonding and Energy Dissipation in a Nanohook Assembly,” *Physical Review of Letters*, vol. 91, no. 16, October 2003.
10. University of Akron News, “UA Synthetic Gecko Foot-Hairs Leading to Reusable Adhesives,” [uakron.edu/news/articles/uamain\\_1293.php](http://uakron.edu/news/articles/uamain_1293.php), Aug. 12, 2005.
11. Liehui Ge, Sunny Sethi, Lihie Ci, Pulickel Ajayan and Ali Dhinojwala, “Carbon Nanotube-based Synthetic Gecko Tapes,” *Proceedings of the National Academy of Sciences of the United States of America*, vol. 104, no. 26, June 26, 2007.
12. Alan Rae, “Nanosolder – What’s Next?” International Conference on Soldering and Reliability, May 16, 2008.

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# Greener PCB COATINGS

Balance cost, performance and environmental impact when selecting a conformal coating. by KENT LARSON

Many of today's circuit boards benefit from the use of protective, yet environmentally "green" conformal coatings that allow them to operate reliably, even in harsh environments. The usage of conformal coatings has been rapidly expanding in recent years, not only in highly demanding applications such as avionics, military and automotive, but also in portable electronics that sometimes face more severe use – and abuse – than you might at first recognize.

Conformal coatings have a proven track record of protecting boards from dust and debris, liquids, and contact with a wide range of harsh conditions that they encounter. Such coatings must protect in very cold to very hot environments, and withstand vibrations and mechanical shocks that range from those encountered in automotive engine compartments to personal electronics that are frequently dropped, kicked, run over, and even immersed in the ocean. In all of these conditions, coatings must protect electronics from shorts and other damage.

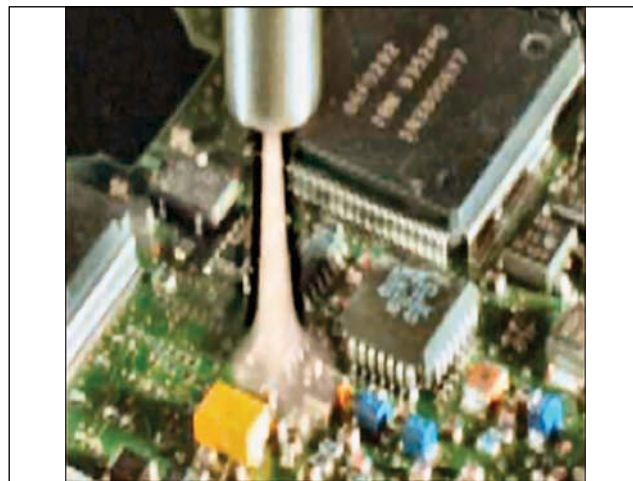
Protective coatings work by closely conforming to surfaces, components, wire bonds and solder joints and forming a barrier to conductive contaminants. Additionally, they electrically insulate and isolate conductors that may be in close proximity to each other. An application of a coating to a PCB is shown in **FIGURE 1**. Conformal coatings are applied at the end of the assembly process, but like the components on the PCB, these coatings are most often selected early in the design process, based on specific performance requirements.

Even with greatly enhanced durability that can come from protecting electronics with a conformal coating, all too often such protection is added as an afterthought or as a last-minute correction to prevent failures brought to light by design-validation testing just before production launch. At this late stage in the game, only limited material characteristics can be considered, and trade-offs between performance, material price and production costs must be made very quickly. Ideally, such durability performance should be designed in from the start.

When improved reliability and durability requirements

lead to coating choices made earlier in the commercialization cycle, designers can not only factor in board layouts that simplify coating application processes, but also consider the potential environmental and material regulatory aspects of their materials choice. There can be considerable differences in the possible environmental impacts of various coatings, and these differences may factor into the decisions of circuit board companies that want to improve the "green" credentials of their electronics.

There are many factors that go into the selection of the best conformal coating for a given application. Cost draws the laser focus of purchasing agents and buyers, and is the bane of suppliers' sales agents. It is easy to concentrate on the price per kilogram of a material when considering various types of coatings, but that is only part of the total cost of ownership. Even materials that meet performance specifications may differ wildly on the cost associated with delivery, inventory, han-



**FIGURE 1.** Conformal coating operation, photo Courtesy: Precision Value and Automation.

dling, dispensing, curing, waste handling, testing, scrap rates and warranty/ reliability/ durability in the final end use.

In **FIGURE 2** the market share for the different types of coating materials is shown. Because of their low purchase price, acrylics are the largest volume coating used, but a low initial cost does not tell the whole story.

A solvent-based coating for instance, may offer a very attractive price per kilogram, but may require multiple application passes to obtain the same cured coating thickness – and therefore level of protection – as a solventless material. Additionally, there are costs associated with shipping, handling, storage, and the use of flammable and often toxic solvents. Moreover these same solvents transform into vapors during curing, and the vapors can often present additional issues to deal with. Also, most solvents are considered Volatile Organic Compounds (VOCs) and, in addition to having toxicological properties, they are recognized as contributors to ozone depletion and/or global warming. Finally, there may be considerable costs associated with the waste disposal of uncured (and sometimes cured) material.

Likewise, materials that require a curing oven not only add capital costs when setting up a production line, but also incur additional energy costs and likely add work for the HVAC of the manufacturing area. Ovens also add cycle time and work-in-process (WIP) costs that must be added to the total cost-of-ownership equation. The example in **FIGURE 3** compares the total cost of two materials. Coating material 'A' had a lower price per kilogram, but ended up with higher processing costs and more rework and scrap costs. When the total cost to coat a board was calculated, the two materials had almost identical cost.

Other factors can include the cost of quality problems, measured by first-time reject and rework rates. On the other hand, improved profit margin in the form of superior reliability and durability for the end product can be achieved and enhanced by making the correct conformal coating selection.

Besides cost of purchase, performance criteria certainly must be met. Even here, just meeting product specification minimum requirements may not be an adequate criterion for choosing one coating versus another. For instance, a minimum coating-thickness requirement must be met to ensure adequate

protection. However, nearly all coating application methods will produce varying thicknesses on a populated board. Vertical surfaces, wires, sharp edges and solder joints often will allow a coating to slump and sag, leaving far less coating and protection in those areas.

Boards may require differing levels of protection, depending on the environment in which they will be used. While board assemblers may try different coatings in pursuing a more perfect match of performance and value for a given application, there are additional costs when multiple coatings are used on a production floor. In some cases, using one product that meets the most demanding requirements for all coating lines may actually incur lower total costs when viewed through the larger picture of an entire plant's operation.

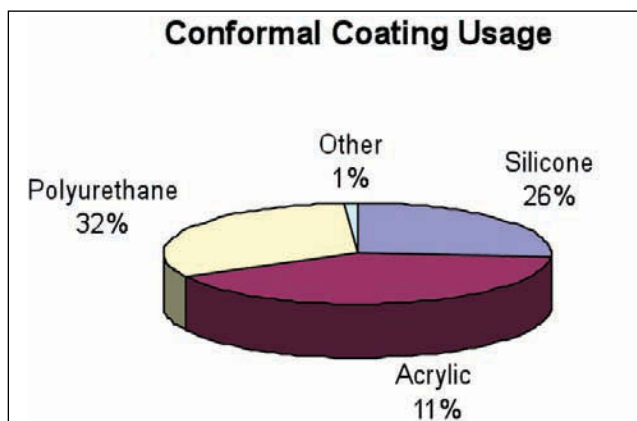
Besides cost and performance, an increasing concern for lower environmental impact is affecting board assemblers' decision making when evaluating conformal coating choices.

**Solvents.** Most production lines capture only a fraction of the solvent vapors given off by many coatings, and this applies particularly to acrylic coatings. These solvents are typically vented to the atmosphere where they are usually counted as greenhouse gases. Additionally, most solvents have noxious odors that are quite objectionable to workers – and to neighbors as well.

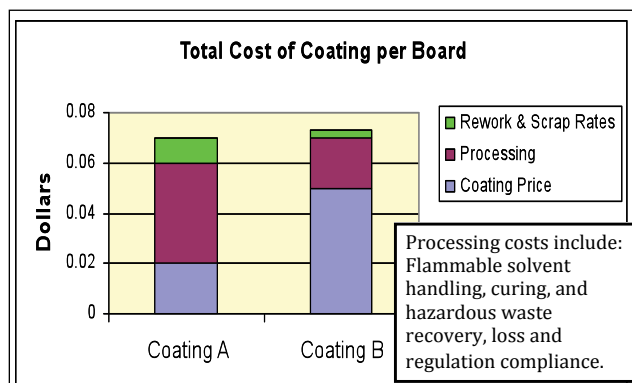
In addition to solvents within the coating formulation, some products, such as parylene, requires an adhesion promotion step that can involve large quantities of solvent that are released into the air and must be either captured or scrubbed before it is vented into the atmosphere.

Solventless coatings create far fewer volatiles or vapors, and therefore may contribute far less to environmental problems such as global warming. Parylene, urethanes and silicones are commonly available in solventless versions. In some cases, silicones are available in solvents that are not considered VOCs or greenhouse gases.

**Toxicity.** While nearly all materials can be considered as having at least some toxicological effects in certain concentrations or exposures, some coatings are recognized as needing greater care when handling, applying, curing and in the disposing of waste materials. Some acrylics and many urethanes can present significant challenges. Parylene and silicone have some of the least issues in this regard.



**FIGURE 2.** Conformal coating market, material type utilization. (Courtesy Prismark Partners LLC)



**FIGURE 3.** The total cost of ownership may be similar between coatings with considerable differences in purchase price.



**Operator Impact.** Besides flammability and toxicology issues, worker exposure to unpleasant or noxious fumes and potential health problems due to skin contact are significant concerns. Parylene, which must be deposited under highly controlled vacuum conditions, is commonly applied only by specialized vendors. Silicones generally are more user-friendly than most conformal coatings.

**Waste.** When considering the environmental impact of a coating, the disposition of the waste associated with its application and use should be taken into consideration. While most spray, flow and dip-tank applications can limit waste to a relatively low percentage, parylene application can generate 90% or greater rates of material waste.

**Environmental Stability.** It is easy to overlook the disposal process of materials once they leave a manufacturing site. Organic carbon-based coatings will last a long time when used within their specification limits, but eventually they will degrade chemically, breaking down with exposure to sunlight, heat, ozone, bacteria and a host of other environmental conditions. Coating degradation causes the release of chemical components into the environment. In **FIGURE 4**, the environmental impact of the various process steps is detailed. Silicones are widely recognized as having far superior stability to harsh and prolonged exposure conditions.

**Environmental Impact.** When carbon-based coatings do degrade, they release considerable carbon-content chemicals into the air and ground, since they are typically made up of greater than 90% carbon. However, since silicones are based on an inorganic mineral-like structure, they have far less carbon to release when they do eventually degrade. Typical silicones have only 33% carbon content (**FIGURE 5**).

Many electronic applications have had to deal with lead-free regulations that have required use of alternative soldering materials. While reducing the potential environmental impact of lead, these regulations have caused other issues. One of the bigger problems has come from the higher tin content in solders. Under some conditions, tin will form “whiskers” and other phenomenon that can bridge between conductors, causing electrical shorts and failures. This has substantially reduced

reliability and life expectancy on some circuit boards.

Several studies have shown that silicones have been one of the best conformal coatings at slowing the formation of tin-whiskers. Additionally, they also may deflect the growth direction, which can prolong the life expectancy of the electronic assembly.<sup>1</sup>

## Conclusion

There are many factors that go into the selection of conformal coatings used to protect circuit boards. Performance is critical, and total cost of ownership must ensure economic viability. Environmental “green” concerns are growing in importance, even in emerging markets at both the corporate and governmental levels. Each type of conformal coating has its own set of benefits and detractors that must be considered to make the best performance, economic and environmental choices.

Acrylics have a very low price, but many contain undesirably high levels of solvents that pose significant flammability, toxicological, and environmental concerns. Their low price may well be offset when looking at the total cost of ownership and environmental impact.

Urethanes offer expanded performance at an intermediate price, but health and safety concerns can seriously compromise their perceived value and the full costs of use. When urethanes degrade, they can release high levels of both carbon- and nitrogen-based chemicals into the environment.

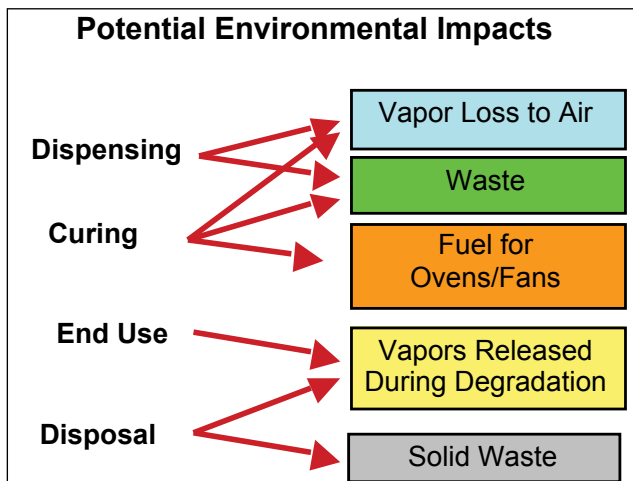
Parylene is a specialty coating whose total cost of use can be extremely high. It also has by far the highest material waste associated with typical protective coating applications.

Silicones have a high purchase price, but their ease of use, high performance, superior stability, relatively low environmental impact, and the increased reliability improvements for circuit boards can often reduce their total cost to the same or even less than other common coatings. **PCD&F**

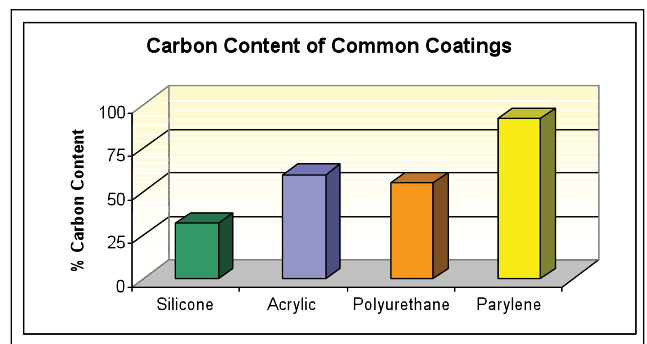
## REFERENCES

1. Evaluation Of Conformal Coatings As A Tin Whisker Mitigation Strategy, Part I & II, Thomas A. Woodrow and Eugene A. Ledbury, The Boeing Company, Seattle, WA.

**KENT LARSON** is a senior engineer within the Electronics Global Application Engineering Center at Dow Corning Corporation and can be reached at [electronics@dowcorning.com](mailto:electronics@dowcorning.com).



**FIGURE 4.** Potential environmental impact areas in the manufacturing process.



**FIGURE 5.** Carbon content of common coating materials.

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# Environmentally Friendly DIGITAL INKJET SOLDER MASK

The advantages of inkjet processing provide the PCB fabricator with a new tool to improve product quality and reduce waste. by YEHUDA DAVID and DR. YIFAT BAREKET

The traditional solder mask process requires expensive capital equipment and a major amount of production floor space, in both the wet process area as well as in the clean-room environment of the “yellow room.” Because of the number of steps, traditional liquid photoimageable solder mask processes involve a high number of skilled employees. The total process involves the use of a number of chemicals (developer) and the manufacture and maintenance of photo tools used to image the solder mask. While today’s solder mask materials are fine tuned, quite often the results demonstrate limited performance, long cycle time and a major contributor to the total “cost of goods” in the profit and loss statement of many PCB companies. The expected benefits from digital inkjet solder mask printing as shown by comparative tests with other systems are numerous and significant, and may include:

- flexibility with balancing line throughput
- higher registration accuracy and resolution
- ability of printing robust solder dams between fine pads
- no solder mask residue inside holes
- adjustable, selective coating thick-

ness for conductors, laminate and power areas

- labor, photo tools cost savings, reduced cycle time and material savings
- reduced chemical waste and waste treatment costs

Inkjet digital printing allows significant simplification in the solder mask process. The one-step process also has the potential to increase final yield in both PCB fabrication and assembly. Handling (and handling related) defects are minimized in the PCB fabrication process, and “selective additive printing” technologies minimize shorts and improve yield in the assembly process.

## Zero Clearance Technology

Using a traditional solder mask process with a medium pitch density SMT component, most PCB manufacturers are able to produce solder dams (used to prevent shorting during the reflow operation) with sufficient clearance between adjacent pads. However, in the case of a high-density SMT component, many PCB manufacturers cannot produce the required solder dams. One limiting factor is that there is insufficient registration accuracy between the film and the PCB in the

traditional solder mask process. Additionally, with many processes there is a resulting solder mask undercut after exposure and development, which reduces adhesion of the mask so that solder dams cannot stand up to further processing. In these cases, where a solder dam is needed for advanced high-pitch components, the industry is often forced to do without, simply because the traditional processes are not robust enough to generate reliable 3 mil or thinner solder mask dams.

These problems associated with traditional processes can be avoided by digital inkjet printing, with each panel going through an individualized registration process between the CAM data and the panel prior to printing, facilitating accurate solder mask deposition, as seen in **FIGURE 1** and **FIGURE 2**.

## A Selective Printing Method

**Holes.** With a traditional process, the solder mask stage is applied as a non-selective coating. Typically, a double-sided screen coater or spray coater applies the solder mask material to cover the entire panel. During this process, not only are the board surfaces coated with solder mask, but the holes are partially or completely filled



with solder mask as well. Removing the solder mask from high aspect ratio via holes and blind vias can be a difficult and sometimes impossible task. These non-cured residues can create numerous problems, which become especially evident during the component assembly process.

Digital inkjet printing, on the other hand, is a selective process that does not fill or coat holes or assembly attachment areas with solder mask at any time, so there is never a chance of residue.

**Traces and Shoulders.** Some experts believe that surface finishing anomalies, such as the “black pad” can be attributed to residue on the copper surfaces from incomplete solder mask development. In the traditional process, conductors are not always symmetrically covered, and the resulting “thin knee” areas can break down, allowing solder to bridge across traces resulting in shorts after the assembly process.

Digital inkjet printing, on the other hand, is a selective process the desired thickness of solder mask is selectively applied to the board with a proprietary coating technology that results in a symmetrical coverage of conductors, even traces that result from high copper thicknesses, using less material than the traditional methods, with a corresponding savings in material cost. (FIGURE 3)

## Solder Mask Formulation Challenges

The solder mask has a number of functional requirements after application to the PCB. Chemical formulation is key

to the cured solder mask material final properties. According to IPC-T-50, this layer is considered “a heat resistant coating material applied to selected areas to prevent the deposition of solder upon those areas during subsequent soldering.” The chemical, physical and electrical properties of this micron-scale coating are carefully detected and the final material quality should meet the IPC-SM-840D standard.

The common UV cured solder mask formulations are always a mixture of various ingredients, composed by several chemical groups, each of them added for specific purpose. The primary ingredients are as follows:

**Resins.** A combination of monomers, oligomers and polymers with varying chemical structure and performance, responsible for determining viscosity, basic rheology, adhesion and the dried film chemical and mechanical properties.

**Fillers.** A combination of inorganic particles, various surface treatment performance enhancing ingredients, and organic particles used primarily for ink stability, opacity, color, and the mechanical and electrical properties of the dried film.

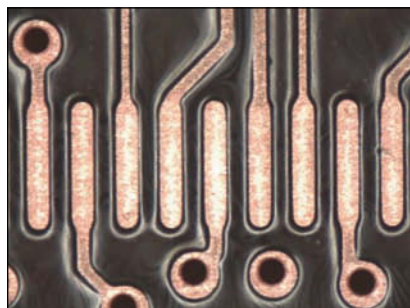
**Surface-active elements.** A combination of surfactants including charge properties as well as basic hydrophobic and hydrophilic moieties for ink stability properties via particles stabilization.

**Additives.** Special ingredients such as an antifoaming agent, leveling agent, flame retardant, biocide, etc., are incorporated for both wet ink performance as well as the dried film properties.

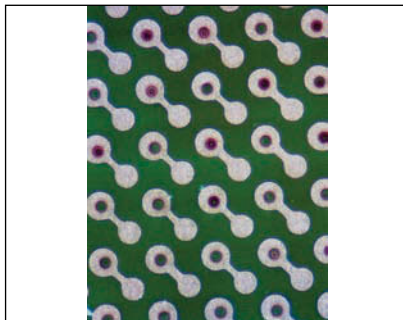
Each one of the conventional application methods such as screen printing, spray or curtain coating requires different solder mask viscosity i.e. from liquid to past form. In addition, the particle size of the fillers in these formulations often have little effect on the overall performance of the coating.

The digital inkjet solder mask printing technology needed to reevaluate the standard solder mask parameters. All the traditional criteria were taken into consideration in the formulation of a new type of solder mask that was tailor made for both the application specifics of inkjet deposition and one that embodied both UV and thermal curing ink properties to facilitate productivity. The demands from inkjet solder mask ink properties are much more complicated than those described above for a traditional solder mask material. The task of optimizing the deposition characteristics and retaining the excellent film properties was paramount. The major differences between the approaches are as follows:

**Inkjet solder mask ink viscosity.** For inkjet technology, the ink viscosity is a major factor. The ink delivery system starts from a main container, continues to a middle container and ends at the print head system. In order to obtain continuous ink flow without blocking a passageway, it is essential to keep the ink at a remarkably low viscosity, usually 10-20 cps at the jetting temperature. This unusually low solder mask ink viscosity is achieved by the careful selection of resins. Maintaining viscosity, while keeping the other properties, such as curing



**FIGURE 1.** Zero solder mask clearance around pads by digital ink-jet printing technology.



**FIGURE 2.** Higher registration accuracy and resolution.



**FIGURE 3.** Selective added solder layer over conductor and holes free of solder by digital ink-jet printing technology.

efficiency, exactly the same, was a challenging task. The new formulation performs to the required industry standards, as well as having other essential production favorable characteristics compatible with the inkjet process.

**Ink particle size and distribution.** For inkjet inks, the filler particle size is critical for print head performance and maintenance. Solder mask ink must exhibit an average particle size in the sub-micron range, with a very narrow particle size distribution. This property is common for inkjet inks but is definitely unique for inks used in solder mask material.

In order to achieve this feature while keeping other essential properties, suitable raw materials must be selected as well as applying an effective grinding procedure. Minimizing ink particle size requires the addition of unique surfactants to ensure consistent ink performance. It should also be emphasized that both previously mentioned parameters are theoretically contradictory to each other, since particle size reduction tends to increase the mean viscosity.

As a result, the inkjet solder mask is a sophisticated formula that contains a high solids content with nano to micron scale particles, while maintaining very low viscosity suitable to the jetting parameters, with desirable dried film properties comparable to other industry accepted solder mask materials.

Another important factor for solder mask performance is its curing system. The inkjet solder mask ink uses two

curing systems, a UV and a thermal initiated cure. This hybrid, patent pending formula integrates the benefits of each system, precisely adjusting the performance to meet the demands of the digital inkjet environment.

Considering the environmental benefits of the digital printing solder mask process, both machine and compatible ink offer an ecologically friendly approach to the development and production process. The ink ingredients were carefully selected to minimize VOC and other irritating or harmful components. The formulation is RoHS approved and the dry film passes UL 94 V-0 grade.

The PCB industry is moving aggressively into the age of digital printing, with the adaptation of inkjet printing for imaging, solder mask and legend inks. In some applications, inkjet will also be used to selectively build circuit traces with an additive application of conductive materials. The operational benefits of these systems are clear. The technological advantages that can be achieved by digital solder mask printing will have a major impact on the future of the PCB industry. **PCD&F**

**YEHUDA DAVID** is the product manager of Greenjet and Dr. **YIFAT BAREKET** is vice president – chemistry for Printar Ltd. They can be reached at [yehuda\\_d@printar.com](mailto:yehuda_d@printar.com) and [yifat\\_b@printar.com](mailto:yifat_b@printar.com) respectively.



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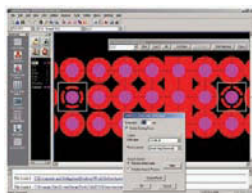
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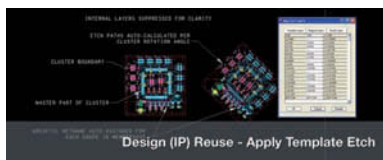


### CAM TOOLS

DownStream's CAM350 Version 10 features integration with Blueprint's document authoring software to create and distribute the files required for a PCB fabrication and assembly release package, resulting in a single file for PCB post-processing. The product can be used in the verification of design data prior to PCB fabrication and allows users to distribute, view and extract documents, Gerber files, NC Drill/Mill data and panel designs for the manufacturing process.

**WHO:** Downstream

**WEB:** [downstreamtech.com](http://downstreamtech.com)



### LINK LAYOUT TO SCHEMATIC

DesignAdvance Systems, Inc., releases CircuitProbe, which enables bi-directional communication, through IPC, between layout and a PDF of the schematic. The tool gives designers and engineers the ability to select design elements in either Cadence Allegro Viewer environment in or a PDF of the schematic, with the corresponding design elements selected in the other application.

**WHO:** DesignAdvance

**WEB:** [ema-eda.com](http://ema-eda.com)



### PTFE MATERIAL

RT/Duroid 6202 PR, PTFE material produces resistor tolerances claimed to be as low as 5% for high reliability planar resistor applications. Additional embedded resistor products offered by the company include RO4003C and RO4350B laminates. The products are produced for use with thin film embedded resistor copper foil in high-speed electronic devices and enhanced copper bond technology for cost-effective performance and reduced PIM.

**WHO:** Rogers Corp.

**WEB:** [rogerscorporation.com/acm](http://rogerscorporation.com/acm)

## OTHERS OF NOTE

### BOUNDARY-SCAN TESTER

JT 2147/AGP is for use with Aeroflex in-circuit testers (ICTs), allowing the 4200 Series systems to be interfaced with JTAG's boundary-scan controller. The product allows boundary-scan test access port (TAP) signals within the ICT system for claimed improvement in signal integrity and a simplified design. The company claims that the product can be installed on the Aeroflex GPIO custom interface module to provide ground isolation plus a switching matrix to route TAP signals to pins on the test fixture. Benefits include fixtureless test preparation and the re-use of stand-alone applications such as prototyping and field service, with increased cost-effectiveness through reduced test fixture complexity.

**WHO:** JTAG Technologies

**WEB:** [jtag.com](http://jtag.com)

### INKJET CONDUCTIVE SILVER INK

Sunjet, has announced the development of silver nano-particles ink designed for conductive films. The company has partnered with manufacturer of nano-particle silver, to allow claimed dispersing of the silver particle products at near 20 and 40 weight percent silver content. The company claims that the inks can be sintered at very low temperatures, below 150C, which is critical for some printed electronics applications.

**WHO:** Sunjet

**WEB:** [sunjetink.com](http://sunjetink.com)

### MIXED SIGNAL TESTER

ABI's BoardMaster 8000 PLUS diagnostic system is used in the testing and diagnosis of analog, digital or mixed signal PCBs. The system allows users to store instrument settings, test procedures, measurements and results for a known good PCB, then runs an automated test to compare test PCBs, highlighting any faults and their locations. The company states that the product is PC controlled, with five ABI instrument modules (standard), and features include digital and analog IC testing, digital oscilloscope, digital multimeter, function generator, frequency counter, variable power supply and universal I/O.

**WHO:** ABI

**WEB:** [abielectronics.co.uk](http://abielectronics.co.uk)

### THERMAL IMAGING FOR PCBs

OptoTherm's new EL thermal imaging system enclosure provides a claimed stable test environment from the ambient environment, blocking air currents generated by heating and air conditioning ducts that can influence the thermal patterns shown by its infrared camera inspection system. A motorized camera slide and controller position the camera for circuit board comparison and short circuit tests, and to verify PCB functionality. A platform with adjustable PCB locators enable repeatable positioning of board sizes up to 22" x 20".

**WHO:** Optotherm

**WEB:** [optotherm.com](http://optotherm.com)

### FREE PCB LAYER STACK EDITOR

LKSoft 2nd edition STEP-AP210 (ISO 10303-210) Electronic Assembly Interconnect and Packing Design used to coordinate information regarding PCB procurement, design and fabrication and to standardize data exchange. The company claims that tools for converting, viewing and editing of CAD/CAM data in the areas of mechanics (2D/3D), electrical installation, printed circuit boards and assembly, and the connecting of this information with PDM and PLM systems is included with the product. The free 90 day license in June and July 2008, extended to a full year if you provide feedback.

**WHO:** LKSoft

**WEB:** [lksoft.com](http://lksoft.com)

### SENTINEL-PI DESIGN SOFTWARE

Apache Design Solutions' Sentinel-PI chip-package-system design and analysis software allows SoC-Aware modeling and analysis of power delivery network for IC package and PCB designers. The company claims that the product allows 3-D full-wave power network extraction and integrity analysis for package and PCB designs, as well as resistance check, static IR-drop analysis (DC) and frequency-domain simulation, and impedance analysis of multi-port power delivery network of the chip, package and board (AC), and time-domain dynamic voltage drop analysis (transient).

**WHO:** Apache Design Solutions

**WEB:** [apache-da.com](http://apache-da.com)



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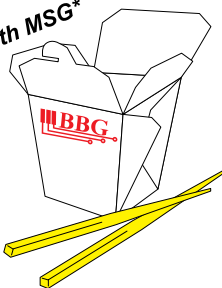
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*BGA Bulletin, continued from p. 48*

**The Diagonal Region.** The pins along the diagonals could have conflicting patterns when the Region 1 and Region 2 fanouts merge. The example in **FIGURE 6** shows a method that not only merges the patterns, but also spreads the vias away from the centerline, providing greater route density along the diagonal.

Dividing up the BGA into regions enables maximum route density, and can thereby reduce the number of layers needed. When the BGA has over 1500 pins, simply routing out of the BGA tends to be the primary contributor to increased layer count. By varying the number of rows used in each region, based on the stackup and via spans available, you can obtain the most optimal fanouts and routing in the context of your own specific design. **PCD&F**

**CHARLES PFEIL** is an engineering director for Mentor Graphics, Systems Design Division. He can be reached at [charles.pfeil@mentor.com](mailto:charles.pfeil@mentor.com). Go to [www.mentor.com/go/bga](http://www.mentor.com/go/bga) to obtain a copy of Charles Pfeil's new book, "BGA Breakouts & Routing."

# Routing BGA Fanout Patterns by PCB region

Routing high pin count BGAs contributes to increased layer count, but maximizing route density by region using blind and buried vias can reverse the trend.



CHARLES  
PFEIL

**THIS ARTICLE PRESENTS** a new concept in applying different types of fanout patterns for BGAs by specific region. The figures in this article show the overall view of the BGA and the regions, along with detailed views of the fanout pattern in each region.

The reason for using regions is to get the most effective fanout patterns based on the available via spans and layer stack-up. The idea is to fan out with layer 1:2 and 1:3 blind vias around the perimeter of the BGA using an aligned-via pattern (described in detail in previous articles) thus effectively reducing the size of the BGA that must be routed using buried or through-vias.

This technique can be applied when blind and buried vias are available. The exact pattern used in each region will likely vary depending on the balance of the route density, signal, and power integrity requirements. The fanout patterns and the regions in this example focus on maximizing the route density. We will look various

patterns based on the stackup and via spans in **FIGURE 1** and demonstrate how variable depth microvias can be used.

**Region 1** comprises the outer rows. The number of rows will vary from 4 to 6, depending on the design rules. As shown in **FIGURE 2**, this region uses a 1:2 microvia with the intent of routing the traces on Layer 2 at maximum route density. This pattern can be varied by moving the via closer to the ball pad and changing the angle, so that the via spacing exceeds the minimum. If you do this, the route density will decrease; however, you may increase room for plane fill and reduce potential crosstalk between the vias.

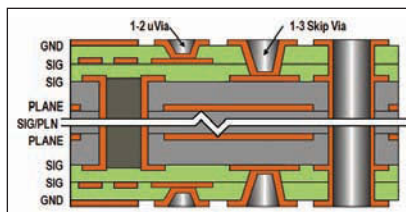
**Region 2** includes all the inside rows. Once the outer rows of BGA pins are routed using the 1:2 micro-vias, the next 4 to 6 rows should use the 1:3 skip-vias, with the intent of routing the traces on Layer 3 at maximum route density, as shown in **FIGURE 3**. Using the skip-via allows a connection from Layer 1 to Layer 3 without a pad on Layer 2. This pattern can also be varied by moving the via closer to the

ball pad and changing the angle so that via spacing exceeds the minimum.

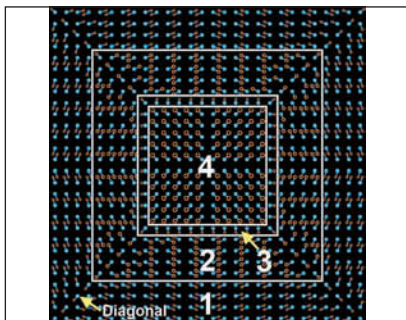
**Region 3** is the transition between the inside rows (Region 2) and the center rows (Region 4). Since the patterns between Regions 2 and 4 will usually conflict and cause DRC violations, a transition area is appropriate. **FIGURE 4** shows a useful pattern for the transition area. A 1:2 or 1:3 via can be used in the transition area depending on your routing strategy. In this example, the pattern is a simple orthogonal short dog-bone. Other angles may be used depending on the via size used.

**Region 4** is the center. The center rows are those left over after other regions have been defined. Usually, the center of the BGA has power and ground pins, and thus putting the through vias in a standard dog-bone pattern as shown in **FIGURE 5** makes sense. Note that the vias are not located in the exact center of the ball pad matrix – this allows for a greater ground plane fill on Layer 1.

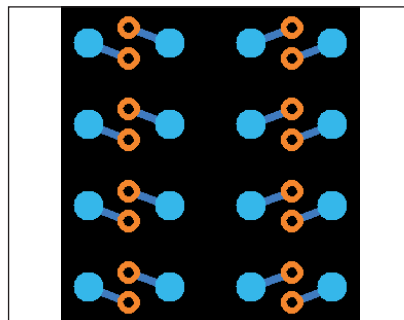
*Continued on p. 47*



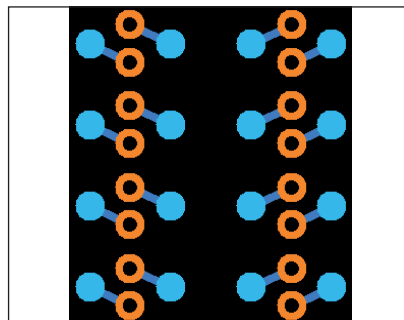
**FIGURE 1.** Lpc type ii hdi construction.



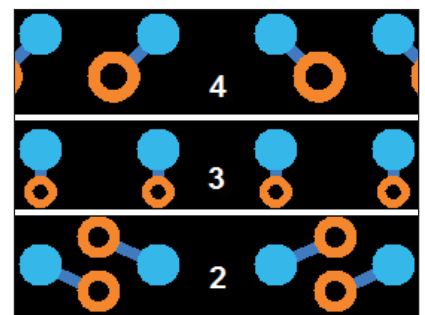
**FIGURE 2.** BGA regions.



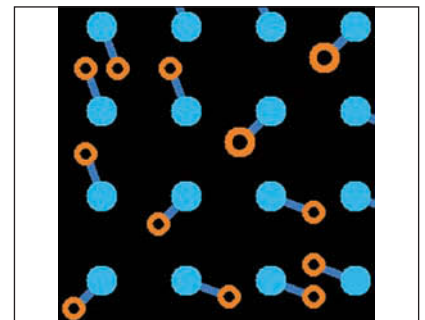
**FIGURE 3.** Region 1 via pattern.



**FIGURE 4.** Region 2 via pattern.



**FIGURE 5.** Region 3 via pattern.

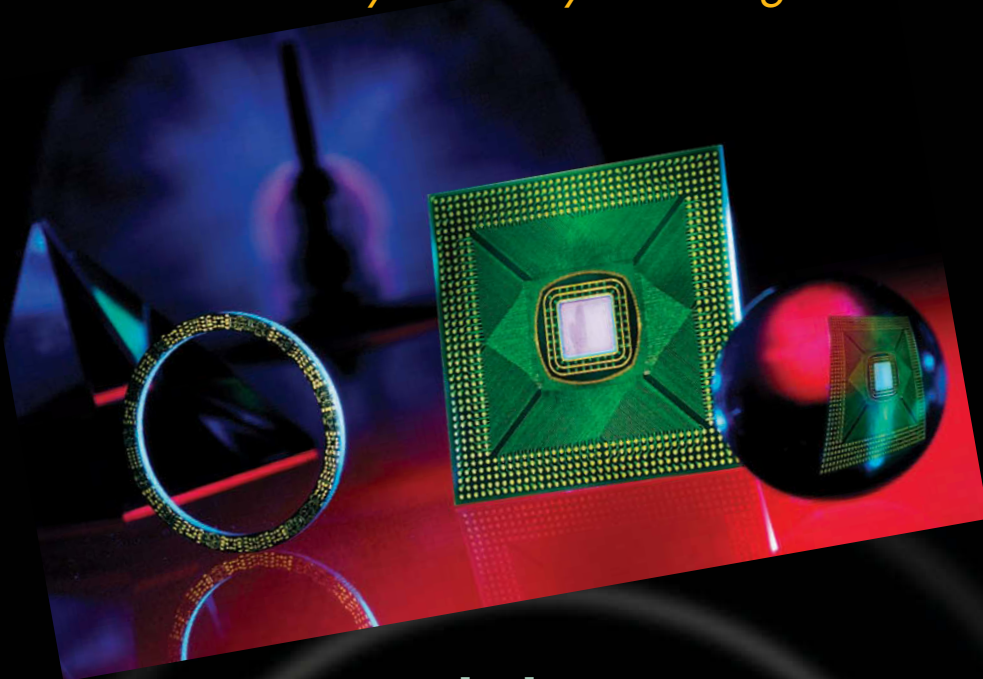


**FIGURE 6.** Routing in the diagonal region.

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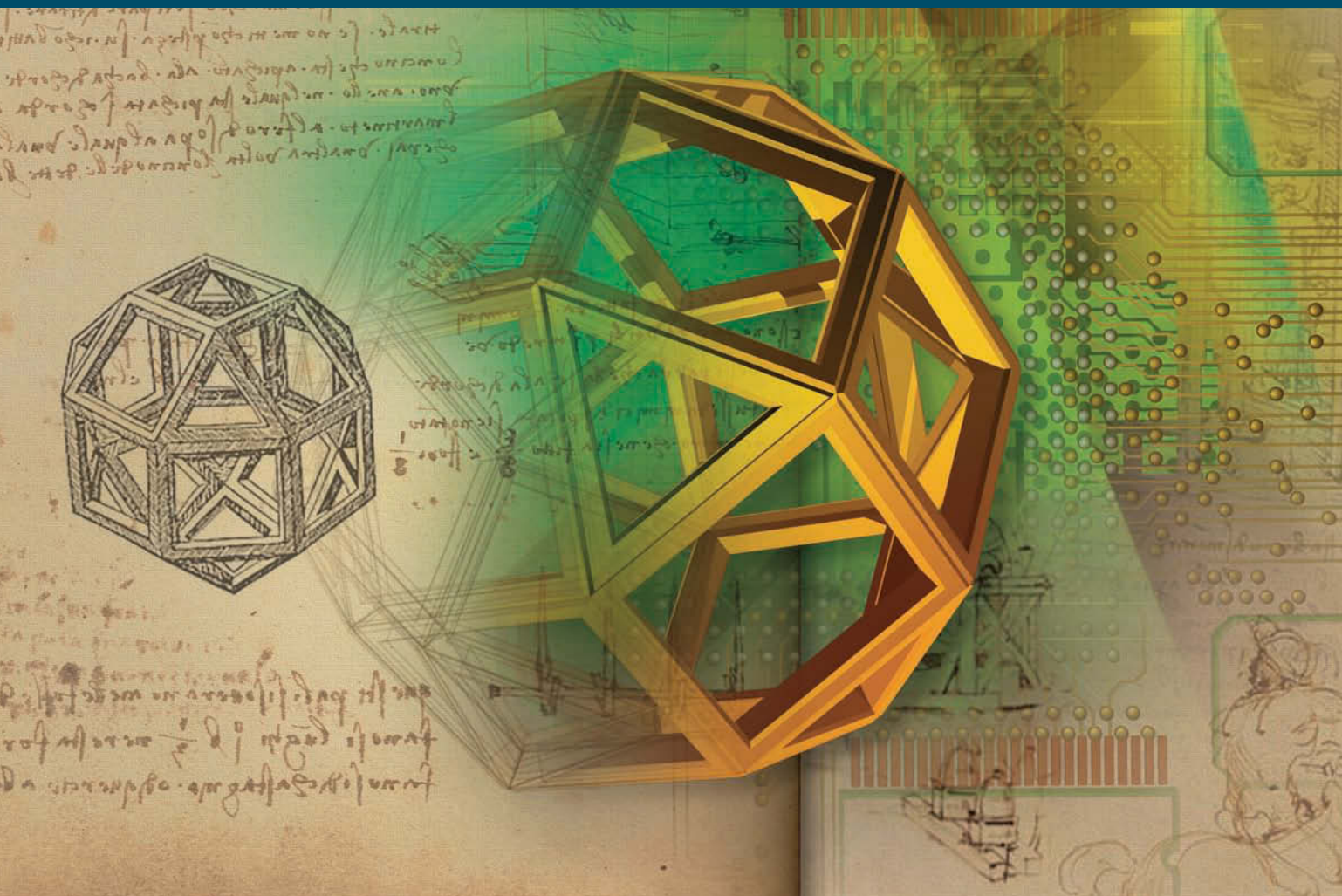


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