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Avoiding EMI In Capacitive Touch Screens

Capacitive touch is now the technology of choice for high end consumer applications but the technology is particularly susceptible to EMI. Sally Ward-Foxton asks how do major manufacturers deal with this problem?

Touch screen technology has been incorporated into practically every consumer device with a screen, from the large display of the iPad down to the smallest digital camera or GPS screen.

Millions of devices integrate touch technologies, employed to create interesting user experiences utilising touch, multi-touch and gesture recognition.

Capacitive multi-touch technology is the most widely adopted technology in these high end consumer devices as it promises a raft of benefits over its competitors. However, the technology does face some technical challenges.

One of the biggest challenges is that of EMI: there are many sources of electromagnetic interference around and capacitive technology is particularly susceptible.

The most commonly cited noise source is from the LCD itself, which of course is permanently in close proximity to the touch sensor. Every LCD panel is different and noise produced by LCDs has a correspondingly wide range of intensities. OLEDs, by comparison, are thought of as a noise friendly choice.

Charging devices are another common source of noise. Since the standardisation of mobile phone chargers to use micro USB, manufacturers no longer have control over the quality of the charger that is plugged into their touch screen mobile phone, and unqualified chargers can introduce significant noise.

So how do high end touch controller manufacturers mitigate EMI in their products?

Superior algorithms

Atmel recently released the maXTouch mX122E series of capacitive touch controllers optimised for 2.8 to 3.5in touch screens such as digital cameras and GPS devices.

They allow up to four simultaneous touches, a level of performance previously seen only in the smartphone market.

Touch processing rejects unintentional touches caused by a gripping hand whilst they interpret light touches correctly for gestures made on the device. The part can support a narrow passive stylus input even when the user’s hand in resting on the screen in a natural writing position.

Atmel says these devices deliver the most advanced signal processing and algorithms to mitigate noise from after-market chargers and other sources.

“The common technique to guard against display noise is to add in a physical shield layer between the sensor and the display, which adds both cost and thickness to the design,” explains Helen Francis, Atmel’s Senior Marketing Manager. “With noise processing on Atmel’s
Atmel’s maXTouch mXT112E allows up to four simultaneous touches, a level of performance previously only seen in the smartphone market.

For many competing solutions RF noise is also a challenge,” she adds. “However, the Atmel touch screen controller operates outside this frequency range, so this is easily avoided.”

Maxim has developed the Max11871 as part of its Tac-Touch series which, it says, has such a high dynamic range that it can detect even a touch from a gloved hand, which is notoriously difficult for capacitive touch. This product can detect and track up to a ten finger simultaneous touch.

Maxim says the Max11871’s analogue front end is built from the ground up for capacitive touch by the company’s high resolution data converter IC design team, and provides a near 60dB signal to noise ratio performance.

Maxim’s Max11871 provides near 60dB SNR performance, a 1000:1 equivalent ratio between touch and no-touch.
which is equivalent to a 1000:1 ratio between touch and no-touch. This is said to be some ten times more than existing products.

“Noise is the number one problem for our handset customers [when selecting a capacitive touch controller],” says Bart DeCanne, Business Director for application specific data converters at Maxim. “EMI immunity is really a problem of dynamic range: you want to detect a weak signal, like a touch from a gloved hand or stylus, in the presence of a large noise. Most touch controllers on the market have a broadband analogue front end controller but you need to scale back the gain of the front end controller or it will be overloaded [with noise] and the weak signal will be lost.”

Maxim’s impressive SNR enables detection of very weak (in the femtofarad range) touch variations, such as from a hand waving near the screen (proximity detection), touch from a fine tip stylus or ballpoint pen, or a gloved hand. Also, it means that the touch point can be further away from the sensor, allowing for thicker cover glass for improved ruggedness.

“We also have a system which rejects noise at frequencies other than the frequency we accept from the touch screen,” he says, referring to the Max1871’s proprietary architecture that rejects noise (by over 40dB) from external sources such as AC USB chargers, LCDs, or CFL lights.

**Frequency hopping**

The STMicroelectronics solution to display noise is based on synchronising the acquisition of touches with the display blanking time. And the company’s latest multi-touch controller, FingerTip, provides both frame and line sync methods. This single chip solution is for touch screens up to 10in diagonal and features a 32bit DSP engine to help drive its EMI immunity.

The company also cites conducted noise from chargers, present on both power supply and ground, as a problem since it creates false touches. Giuseppe Noviello, Director of Technical Marketing for the STMicroelectronics Sensor Business Unit, says that false touches can also result from noise injected by the user’s fingers touching the panel. “In the case of finger noise,” he says, “it is the human body that captures radiated noise, like the noise generated by fluorescent lamps or coming from other low frequency (below 1MHz) sources and transfers it to the screen. There is no easy countermeasure because it is in the same frequency range as the panel touch acquisition circuits and even if it’s periodic, it is affected by wide jitter and most of the time it is modulated.”

According to Noviello, the common solu-
tion for conducted noise is based on frequency hopping and a heavy firmware heuristic algorithm to eliminate suspected false touches. Using the MCU to create filters can reduce or eliminate the unwanted touches but it will reduce the scan rate and response time. Frequency hopping also cannot deal effectively with noise when there is modulation and jitter.

FingerTip, like other solutions, uses frequency hopping to scan the panel in a noise-free area in the frequency domain. This area may be pretty narrow because of jitter and modulation, causing corruption of the valid signals coming from any finger movement.

FingerTip uses a narrow band digital demodulation method with proprietary DFT filtering that is able to strongly attenuate the adjacent noise component. All the signal processing is done in the analogue front end using a state machine: the processor is not involved so the response time is not affected and the raw data coming in is already filtered to an SNR level that can provide the required accuracy and jitter, even in the presence of tens of volts of noise injected on the panel.

“In order to overcome these limitations,” Noviello says, “ST is adopting a series of techniques that come from its strong know-how in capacitance to voltage conversion already used in MEMS analogue front end design.”

In a MEMS device, the mechanical sensor outputs capacitance variations as low asatto-

Farads \(10^{-18}\)F when the capacitance of the system is a million times bigger. The detection of such small signals requires sophisticated analogue filtering techniques in order to get fast response time with a strong SNR.

“The capacitive touch screen,” Noviello explains, “also sends small capacitance variations created by the finger touch to the analogue signal conditioning circuit. Like the MEMS case, these variations are very small, typically in the range of femtofarads but the panel capacitance to earth is a thousand times bigger. The analogue front end resolution must be enhanced to a significant level for a touch to be recognised, and FingerTip’s ADC and signal conditioning circuits use similar methods to MEMS devices to achieve the best SNR.”

Capacitive touch screen controller manufacturers need to protect against noise of many different types from many different sources.

Advances in design for EMI immunity now allow today’s touch screens to pick out even the smallest signals from an ocean of electrical noise. And manufacturers are continuing to refine their approaches to EMI in capacitive touch and are also introducing new techniques based on their accumulated experience in analogue electronics and MEMS.
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Wireless Access Control’s Weakest Link

Wireless access control is only as good as its weakest link, says Microchip’s Vivien Delport & Cristian Toma.

Designing low cost, secure wireless solutions has been significantly simplified with recent advances in microcontrollers, RF ICs and compact security algorithms. However, wireless design still requires a strong understanding of the latest attack methods used to break security systems. Finding the right counter-measures that are affordable is only possible if the designer takes on a system wide approach to security.

With such a wide range of component and technology choices, designers should not simply look for specific security features on a device datasheet but engage in a detailed discussion of all design options with the microcontroller supplier.

One wireless security solution simply does not fit all applications and various factors need to be balanced if designers are to find a system that delivers adequate, affordable protection. Latest microcontrollers feature advanced security encryption algorithms, on-chip RF communication or low power technology, together with dedicated RF ICs, and can help designers easily develop a complete, secure wireless system that delivers the right balance of cost, size and functionality.

No wireless access control device is unbreakable! It only takes time and money for cryptoattackers to find a way to break the device and read the protected information. With a system level approach to security, designers can develop a powerful arsenal with which to...
protect wireless access control devices. Security is a system wide issue and it is crucial for designers to consider the security of the mobile/transmitter and the base/receiver section of their design, as well as potential weaknesses in their hardware.

Security algorithms
Unless a designer is fully familiar with different types of potential crypto-attacks such as plaintext, side channel, differential crypto-analysis, meet in the middle and slide attacks, choosing a security algorithm can be difficult.

Using a public algorithm such as DES, the data encryption standard, encryption is provided by a 56bit encryption key whilst AES, the advanced encryption standard can use either 128 or 256bit keys. Designers can also use proprietary algorithms such as Microchip’s Keeloq which combines a strong cryptographic algorithm with code hopping.

Code hopping, or rolling code, provides an additional level of security by changing the cipher message each time it is transmitted, this then prevents the re-use of previously transmitted messages.

Unfortunately, higher security often means higher cost. The stronger the algorithm, the more complex the calculations and there lies the need for larger software memory. This typically requires a more expensive microcontroller which adds to the overall cost of the security solution and its complexity.

Stronger algorithms also typically result in longer crypto messages that need to be transmitted. This will add longer time delays and also increase the power consumption when sending the radio packet over the air, because the packet takes more time to send. Longer data transmission is not always desirable and can negatively influence the field acceptance of the product.

Hiding the key
Effective key management is as important as the choice of security algorithm. Kerckhoff’s Principle states that a security system should not rely on the security algorithm being secret but rather on the key being secret. It is always safest to assume that both the encrypted message and the algorithm will eventually be known to the public, even if it is a proprietary algorithm.

System security should, therefore, never rely solely on the algorithm being secret but also consider how the security encryption keys will be generated, exchanged, stored, safeguarded, used and replaced throughout the system to decipher or unscramble encrypted messages.

A critical element of any key management scheme is that not all devices use the same...
secret key. This helps to increase overall system security, so that if a single mobile unit is compromised, it does not compromise the entire security system. The easiest way to implement this is to give each mobile unit its own unique secret code or encryption key.

One method often used to accomplish this is to serialise each unit with a unique number and then base the calculation of the unique encryption keys on this serial number and a master manufacturer’s code. A receiver unit that needs to support multiple mobile units at the same time can then easily use the serial number to derive the encryption key needed to decipher information transmitted from that specific mobile device.

Mobile unit serialisation is typically carried out at the time of production, either by preprogramming the embedded microcontroller with this information before placing it on the printed circuit board or by using an in-circuit serial programming interface to programme the microcontroller after board assembly.

It is essential to protect the encryption keys at all times, including during manufacturing and especially if assembly is carried out by a third party contract manufacturer. It is preferable to provide the contractor with preprogrammed, code protected microcontrollers rather than try to secure a complete production flow against the illegal copying of encryption keys. Most microcontroller suppliers, such as Microchip, provide personalised quick turn-around programming options on all of their microcontrollers. By providing the manufacturer with device serialisation information, they can preprogramme both the application software and serialisation information into the microcontroller during production testing.

A further good way of protecting system security is to make regular changes rather than keeping the same security solution with the exact same security key information for prolonged time periods. Make changes to either the key management scheme, the master encryption code used to derive the unique encryption keys for each mobile unit, or even migrate to next generation security algorithms as they become available.

The downside to change is the loss of backward compatibility but this is a design trade-off that system designers need to evaluate. In these types of designs, an embedded microcontroller makes it easier to implement on the fly changes, without the need for a complete redesign and allowing the same hardware design to be used for different products.

**Hardware security**

Attacks on security systems reach beyond analysing data and trying to perform mathematical attacks on the security system. They also include analysing the application circuit to see if hardware tampering allows access to the secured system. If the receiver’s output simply pulls a digital line high to activate a relay that presents an easy point of attack. Of course, this only works if an attacker can get physical access to the receiver units’ hardware while in use.
Another attack scheme involves analysing the mobile sender units from the physical component side. This involves analysing the actual circuit and applying specification voltages that signal the microcontroller or current starve the application to see if this allows the attacker to read the secured information stored inside the device’s non-volatile memory.

There are also other invasive and non-invasive methods of attack that try to break the code protection locking that has been built into microcontrollers.

With cyber attackers continually trying to devise new threats, component manufacturers are constantly adding more layers of physical obscurity to protect algorithm codes and keys stored in microcontrollers. It is always best to work closely with a microcontroller supplier to understand which devices incorporate the latest tamper-proof circuitry to protect the information stored inside the device.

**RF parameters**

The frequency used will depend mainly upon the application and regulations. For example, in the US, ISM bands are 315 and 915MHz, whilst in Europe, they are 433 and 868MHz.

The distance covered by the radio link is also subject to guidelines. A typical RKE application requires at least 20m and there can sometimes be a maximum distance requirement. In Japan, for example, the maximum covered range is just 5m and this is simply down to tougher RF regulations.

One of the most common mistakes in design is to focus on the maximum transmitter range and forget that the transmitter and receiver are equally important. Good antenna design can significantly improve the reception from a weak transmitter.

The RF modulation scheme and data rate also have a major impact on operational reliability of the radio link. Frequency modulated radio links are typically less subject to noise. However, such technology adds cost. A more advanced radio link adds cost both to the remote unit and to the receiver. However, with today’s advances in integrated RF transmitters, receivers and transceivers, these devices can fall into the same price bracket as low cost hybrid RF modules.

**Managing cost**

Designers need to fully understand what they are trying to protect and then decide on which security solution to use. This of course will affect total system cost in a number of ways.

Using a microcontroller based solution, instead of an ASIC based design, adds flexibility. Microcontrollers enable designers to make changes simply by altering the software. This is also true if minor code changes are needed to support multiple countries’ regulations using the same hardware design.

**Microcontroller selection**

The latest microcontrollers enable easier de-
velopment of wireless products while delivering high levels of security through the use of software blocks that support most of the encryption algorithms in a high level language such as C. This significantly simplifies the development of a secure wireless application, which can easily be tailored to the rapidly changing consumer markets.

Some microcontrollers can reduce design complexity by integrating on-board wireless peripherals. Microchip’s rPIC devices, for example, integrate UHF wireless transmitters for low power RF applications whilst supporting space constrained applications with a small package outline and a low external component count. Other microcontrollers, such as XLP based eXtreme Low Power PIC devices are optimised for low power applications. These XLP PIC MCUs feature sleep currents down to 20nA and provide compatibility with dedicated RF modules for IEEE 802.11 WiFi or IEEE 802.15.4 ZigBee, as well as transceivers and receivers for ISM band applications.

**RF components**

Another significant advance now enabling shorter time to market is a wider selection of integrated RF transmitter receivers or transceivers. These devices help to reduce the complexity of RF design by integrating most of the RF circuitry needed into a single chip.

Next generation RF ICs only need a few basic external components to enable the full implementation of a high performance RF wireless implementation. These devices also typically incorporate an SPI interface for an easy connection to a microcontroller. This MCU then configures the RF radio to the appropriate required settings and sends and receives the demodulated data packets.

Vivien Delport is Director of Applications Engineering Security at Microchip’s Microcontroller & Technology Division and Cristian Toma is Microchip Technology’s Applications Engineer.

More from Microchip

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Shrinking Chip Geometry
For Maximum Return

Recently, two competing chip companies, each producing ICs in high volume, chose significantly different process nodes for new SoC products targeting the same application. How did the two reach an almost identical unit price and which one achieved the best result overall? Shimon Raviv unravels the conundrum.

As semiconductor fabrication technologies continue to advance, the most advanced independent semiconductor foundries are able to support processes ranging from mature geometries such as 0.18µm to cutting edge nodes such as 28nm.

Newer, smaller geometries are understood to carry higher NRE and per wafer costs, while the larger number of dice/wafer results in a favourable unit price after production ramp-up.

Other factors must also be considered, including the cost and availability of suitable IP blocks, as well as the costs to acquire the necessary knowledge and to update the company infrastructure to work at the most advanced nodes. Furthermore, non-engineering factors such as short term and strategic corporate objectives can also have an important influence on node selection.

Competing approaches
The two specialist chip companies described
produce relatively high volumes of ICs, and the devices are divided approximately equally between analogue and digital features.

Company A saw 0.18µm as the optimum technology for its custom SoC. Typically, fabrication at this node is on 8in/200mm wafers. By targeting this node, the company avoided the time and cost to acquire knowledge and IP at finer geometries. There is some sound reasoning behind this decision: miniaturising analogue circuitry for very small process geometries delivers a relatively low saving in terms of die area.

Company A’s view that 0.18µm can deliver a strong combination of dense digital circuitry and competitive analogue circuitry is reasonable.

Company B chose 65nm for its competing chip design. The resulting cost for a 12in/300mm wafer was a little over five times that for company A’s 8in solution. This translates into a price/mm² about double. However, since the 65nm chip was less than half the size of the 0.18µm design, the smaller geometry yields a small advantage. This is diminished, however, when taking into account the higher costs for mask sets and any ROM code changes at 65nm.

Ultimately, the two companies have achieved broadly similar costs per chip. Arguably, company A has realised its product for a lower initial financial commitment.

However, company B’s investment in expertise and infrastructure at 65nm, which should continue to deliver benefits in future product generations, may prove to be a more beneficial strategy in the longer term.

Node selection guidelines

In this example, the 0.18µm process was able to achieve a competitive unit price. The design contained a relatively high proportion of RF and analogue circuitry, and the digital circuitry was already well defined in relation to mature governing standards.

In other applications, particularly for emerging generations of smart products requiring intensive digital functionality integrated on the chip, a more advanced node may present a better option.

On the other hand, it is important to consider the size of the target market, bearing in mind that smaller process geometries require progressively higher production volumes to offset the increased NRE and wafer costs.

All of these factors must be considered, and a decision taken, before the design can move forward, since the target node has an important influence on the choice of foundry. It is vital to select a wafer foundry partner offering the best price and support at the chosen node. Node selection must also be determined before any third party IP is sourced so that the detailed chip design can begin.

Analogue or digital miniaturisation

The relative proportions of analogue and RF to the digital circuitry included in an SoC de-
sign have an important bearing on the economics of migrating to a smaller process node. Since digital feature size reduces according to a square function, halving the process geometry yields features occupying a quarter of the previous die area.

On the other hand, the same change in design rule will yield savings up to 50% for analogue circuit features. Hence, systems containing a significant quantity of analogue or RF circuitry will deliver a relatively small return in exchange for the higher investment and cost/mm² that are incurred at progressively smaller process nodes.

**IP assessment**

For many projects at mature nodes, most or all of the required IP blocks, for example, cell libraries, I/Os and memories, as well as more complex blocks including PCI Express or USB functions, can be provided by the foundry at no extra charge. However, for more advanced nodes, third-party IP is often needed.

Larger semiconductor companies may develop their own functions as required but today, IP is more typically bought on the open market. If the functions needed are not available for the desired node, or if the costs are considered excessive, a less advanced node may be a more viable choice.

As a guide, third party Flash IP blocks for leading edge nodes may cost in the region of $10~30,000, while more complex blocks such as PCI Express functions, USB or advanced memories such as DDR3 are typically priced $100~700,000.

Selecting IP may not be straightforward, particularly for more advanced nodes. It is worth pointing out that the most advanced nodes, generally, do not benefit from a full portfolio of supporting IP, some custom IP development may be necessary.

**NRE & wafer pricing assessment**

The results achieved by the two example chip design projects discussed earlier highlight how differing NRE costs and per wafer prices influence the final unit cost for each die. Table 1 compares the combined costs of NRE and mask set, as well as wafer prices, for currently active process nodes from 0.18µm~28nm. It’s also worth noting that today’s most advanced nodes deliver greater cost benefits at high volumes.

<table>
<thead>
<tr>
<th>Process node</th>
<th>Wafer size</th>
<th>Relative NRE + mask cost</th>
<th>Relative wafer price</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.18µm</td>
<td>200mm</td>
<td>1x</td>
<td>1x</td>
</tr>
<tr>
<td>0.13µm</td>
<td>200mm</td>
<td>2x</td>
<td>1.5x</td>
</tr>
<tr>
<td>90nm</td>
<td>200mm/300mm</td>
<td>4x</td>
<td>2x</td>
</tr>
<tr>
<td>65nm</td>
<td>300mm</td>
<td>8x</td>
<td>3x</td>
</tr>
<tr>
<td>40nm</td>
<td>300mm</td>
<td>15-20x</td>
<td>4.5x</td>
</tr>
<tr>
<td>28nm</td>
<td>300mm</td>
<td>25-30x</td>
<td>6x</td>
</tr>
</tbody>
</table>

Table 1: Comparison of NRE/mask costs and wafer price for foundry nodes.
significantly over 100 million units/yr.

An accurate guide is to consider the most advanced nodes only for projects where very high production volumes are projected and the design contains a large quantity of digital circuitry. For lower volume designs, or where a significant proportion of analogue circuitry is included, a more mature process may result in the lowest cost per unit.

Projected production volume

The relatively easy accessibility of today’s more mature nodes, such as 0.18µm and 0.13µm, can allow fabless chip companies to deliver commercially viable custom chip solutions for lower volume sectors, such as some industrial and medical markets.

Here, the high initial costs of the more advanced nodes can demand production volumes well beyond the total available market in order to become economically viable.

Negotiable factors

Before committing to a node, serious dialogue with potential foundry partners is essential. Better pricing may be available if the foundry is particularly interested in the project: high projected production volumes may allow the foundry to offer one of its more advanced nodes at a competitive rate. Alternatively, foundries may offer lower rates to long-term, high volume customers.

For this reason, foundries tend to favour larger customers. An alternative is to go through a broker or consultant that can provide the benefit of established relationships with the major foundries.

In practice, working through a consulting partner can overcome many of the potential pitfalls that can be encountered when working with an offshore foundry, across cultures and geographical boundaries. With experience, some fabless chip companies may feel that one particular foundry is easier or more reliable to work with than some others. In fact, most foundries are equally reliable provided a mutual understanding can be established.

It’s also important to bear in mind that the chosen process will continue to mature throughout the duration of the project, resulting in improvements in aspects such as IP availability as well as process yield. By the time the project reaches production ramp-up, most foundries can be expected to achieve acceptable yields at the target node. In addition, foundries will continue to develop new process technologies, such that the most advanced process available at the beginning of the project will no longer be the most advanced by the time full production is reached.

Node targeting

There is a case for targeting the most advanced node that is practicable at the time. On the other hand, a profitable result may be achievable at a more mature node. The decision is essentially commercially driven, based on the projected sales volume and target selling price.

Factors including the quantity of funding available to start the project, the level of expertise in the candidate nodes, and the corporate roadmap for future generations of the product also have a critical impact on node selection.

Arguably, today’s mature sub-micron nodes allow fabless chip companies to realise new designs at a relatively low initial cost. On the other hand, choosing a more advanced node may deliver better results in the longer term, for those companies able to bear the higher up-front costs.

Shimon Raviv is Engineering Vice President at EquipIC supply chain.
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Over the past 60 years, Potters Bar based Soundcraft and Studer have steadily grown their dedicated audio mixing console design and manufacturing businesses, with global sales and support networks. Its mixers are designed for live sound, recording, post-production, and TV and radio production.

This production facility is not currently used for a regular, high volume throughput of a stable, longterm product mix. Instead, its role is to produce prototype and low production quantities of a wide range of products as a service to Soundcraft and Studer as well as other companies within the Group, with volume production handled elsewhere. Typically, the facility processes between two and eight new products every month, for example, in-car microphones are currently being prototyped for Harman AKG in Austria. PCBs for these products include components practically invisible to the naked eye.

This high and constantly changing product mix creates complex issues, especially when some of the products are for sister factories with their own part numbering systems. Speed and flexibility are needed on the production lines to facilitate rapid product changes. To avoid bottlenecks, any test and inspection facility has to be equally as fast and versatile. When Soundcraft Studer’s x-ray inspection system’s lack of these attributes became an issue, automated optical inspection, AOI, looked promising and so the company invested in a Nordson YesTech BX benchtop AOI system.

**Adopting AOI**

AOI is fast, delivering cost-effective quality control compared to in-circuit testing. Once a system is programmed with the component, layout, orientation and soldering information, its strategy of inspecting by comparison to a library of parts and packages allows rapid
throughput of boards during production. Equally essential to Soundcraft Studer, however, was the BX’s ability to be quickly reconfigured and even reprogrammed fast enough to keep pace with different area’s demands for inspection resource.

As the company adopted the BX system, it found that the time needed for programming new boards was heavily influenced by the availability of component data. Lead times for new programmes were reduced as the component library developed and grew. Developing this component library called for careful management of the part numbering for these components, as up to three numbers related to each one: the original manufacturer’s part number; the part number assigned by Soundcraft Studer and if applicable, the part number assigned by the relevant sister company.

As with any AOI system, other parameters apply to each part too: board reference; its X and Y co-ordinates; orientation and package code. These, however, are available from the CAD files used by the pick&place machines. Accordingly, the company built a spreadsheet database that integrated CAD data with part number information, together with storage location. This comprehensively defined each component used in PCB production and integrated with the BX library database.

**Operating experience**

As the database has been growing, set-up times for entire boards have got faster. For example, a board was programmed within 25min of receiving the CAD data even though it contained 123 new components not yet in the...
library. After set-up, inspection has proved to be fast too. An inspection of a double sided board after solder pasting took 23s to determine that the board was ready for soldering. Component presence and position were checked.

The machine also uses OCV to check polarity for each component and also that it is the right part by reading its label. Another useful feature was the AOI’s ability to check component height above the board, as an over-height component could indicate a problem such as a smaller part trapped beneath a BGA being inspected. A further 23s inspection after reflow was sufficient to check for shorts, dry joints, lifted leads and other solder faults.

Soundcraft Studer mounted its AOI benchtop machine on a trolley so it can be rapidly moved to any point in the production line where inspection is required. This is a significant improvement on the earlier situation in which inspection was performed by an x-ray machine permanently in position after reflow. And with just x-ray inspection, it was not possible to detect incorrect components or orientation, and solder is often masked by components in the same position on the top and bottom.

Batch sampling has proven to be well worthwhile with the new system as it can catch problems within the manufacturing process that go beyond a single board failure.

With smaller batches 100% inspection is best as, for example, it is possible for a component reel loaded into a pick&place machine to be populated with mixed components when kitsing small lots. This fault would not be visible, and the pick&place machine would be unable to detect it as it only reads the barcode label on the reel which would probably be as expected.

However, a series of boards rejected by the AOI system for the same ‘wrong component’ failure would soon alert an inspector to the existence, nature and source of the fault.

Two months down the line following installation and Soundcraft Studer has found the AOI to provide the inspection resource essential for its low volume, high mix production environment. Dave Birtwistle, SMT Team Leader at Soundcraft Studer says, “We appreciate the benchtop system’s agility as well as its speed, as this allows its rapid reconfiguration for different product types and process stages, and it is easy to program as well as fast in operation. Above all we can report that to date it has found every fault it has encountered!”

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smart metering

Building A Smarter Meter

The move to smart energy brings massive opportunity across the supply chain but choosing the right solution needs careful consideration at every level, says ByteSnap Design Director Dunstan Power.

As consumers become more aware of energy management, the need to accurately measure and react to energy consumption becomes greater. Evidence of increased energy awareness is all around us, in public places, commercial buildings and our own homes. The need for greater control over utilities such as gas, water and specifically electricity, has led to the emerging concept of smart energy and the smart grid. The active management of energy consumption is a core element of the smart energy concept and delivering this management requires an effective means of monitoring energy consumption.

Measuring energy usage isn’t fundamentally difficult but creating a robust infrastructure around smart energy requires many elements to come together. The underlying technology is developing rapidly to enable the smart grid and the physical devices put in place over the next three to five years will need to remain in operation for many more: up to 20 years and possibly longer.

Against today’s fast moving technological landscape it would be difficult to imagine many electronic devices that would stand that test of time but smart energy measurement and control solutions have to meet this challenge.

Trends within the industry strongly indicate that wireless communication between energy aware devices promises the most viable solution in terms of longevity and functionality. And this is reflected in the efforts of the ZigBee Alliance which has worked co-operatively to develop the ZigBee Smart Energy Standard, now widely trialled by utility providers around the world in preparation for large scale roll-out.

As this roll-out begins, demand will rise for systems that implement the Smart Energy Standard. In parallel to ZigBee certification, these solutions will also need to meet the commercial requirements of a competitive market. To address these needs ByteSnap Design has developed and launched the industry’s first ZigBee
Smart Energy module which integrates metering and control functions in a single, ZigBee compliant platform.

ZMM-01 provides a pre-integrated and pre-certified solution targeting OEMs and system integrators looking for a cost-effective solution to implementing a smart energy solution based on the ZigBee Smart Energy Standard. Using industry leading discrete solutions from Ember and Cirrus Logic, ZMM-01 enables system integrators to bring solutions to market faster and with significantly less development expenditure.

Creating a robust wireless connection is inherently difficult and gaining compliance testing for a wireless device can be both expensive and time consuming. The ZMM-01 removes this pressure by delivering a fully integrated and compliant platform on which to build smart energy solutions. By implementing metering and control functionality on a single module, system integrators are able to target a range of applications where the ZigBee Smart Energy protocol will be used.

The modular design overcomes two significant development challenges: developing a rugged analogue front end, AFE, for measuring mains levels of voltage and current with creating a reliable radio interface implemented using the ZigBee protocol over the underlying IEEE 802.15.4 layer.

The AFE is a Watt/hour meter on a chip, developed with smart energy metering in mind. The AFE accepts two current and two voltage inputs, with an energy linearity of ±0.1% of reading over 1000:1 dynamic range. RMS voltage and current calculations are made on-chip, giving active, reactive and apparent power/energy data with system level calibration and phase compensation. The device meets the IEC, ANSI and JIS accuracy specifications and also provides voltage tamper correction and a power supply monitoring function.

Based on the Arm Cortex-M3 core, the ZigBee SoC from Ember delivers ample processing power and memory bandwidth for the implementation of customer specific applications. Bespoke customisation is enabled though ByteSnap’s ZDM-01 development kit which provides the perfect development platform for end products based on the ZMM-01 module. It includes an optically isolated USB serial port as well as a mains load simulator, giving the ability to vary the current, voltage and phase angle without working with the mains.

Energy measurement and control are intimately linked functions of the smart energy concept: ZMM-01 is the only solution that successfully combines both in a cost-effective, low power platform, says ByteSnap. The potential for smart energy measurement combined with control is only just being explored and as such, ZMM-01 is at the sharp end of integration, providing a flexible wireless platform that can be configured to meet today’s requirements whilst providing the required reliability and robustness to remain in service for many years to come.
Holistic Approach Is Beacon For Waterproof Connectors

Intelliconnect’s new range waterproof connectors were conceived, says MD Roy Philips, when a Personal Locator Beacon manufacturer presented a problem that no one else had managed to solve.

When a market leading manufacturer of personal locator beacons, PLBs, was faced with a problem when military aircrew were using its beacons, the company called in Intelliconnect to help solve the problem. Simply, the problem arose in a non-functioning beacon when crewman had exited the aircraft or boat. But tracking down the problem proved difficult to understand as, like any other piece of emergency equipment, these PLBs were subjected to rigorous testing during manufacture and also a further full functionality shake-down test prior to the manufacturer despatching the equipment.

A thorough investigation of the way the beacons were being used was undertaken, and the problem finally identified by Intelliconnect. Prior to the aircrew bailing out of an aircraft, they would be inclined to twiddle with the PLB antenna and in some cases accidentally disconnect it from the beacon. On bailing out, the PLB would then fill with seawater, leaving the crew member wondering why rescue took longer than anticipated. With the PLB full of water its ability to transmit its location was severely limited and in some cases could even cease to operate.

So the challenge was set in providing a mated pair of connectors that would be waterproof to minimum IP68/NEMA 6P ratings for up to 20m immersion for a minimum period of four hours unmated. And as usual with Intelliconnect designs, the company took its holistic approach, with the complete system investigated.

To provide a sealed connector, complete with modularity and ease of assembly, a TNC to MCX adaptor was designed by Intelliconnect. This enabled a separate umbilical link to be used inside the equipment which greatly improved the flexibility of the manufacturing process. The mating half needed careful consideration, says the company, as the personal locator beacon had to be used in confined spaces. So a low profile, TNC right angled plug, also sealed to IP68, needed to be developed.

A further part of the design brief required In-
telliconnect to take into account the need to attach additional GPS and transmitting antennas without them being connected, inadvertently or otherwise, to the wrong ports. For this requirement, a solution was developed using standard and reverse polarity TNC connector designs that would clearly indicate if attempts were made to wrongly connect them.

The final part of the system to be protected was the battery connector. By using the experience and knowledge gathered on the antenna connector design, it was a relatively simple task to apply this know-how to Telliconnect’s Nim-Camac connectors and also seal them to achieve the necessary IP68 rating unmated.

The resultant Telliconnect solution emerged from the company’s holistic approach to solving the problem, says the company, rather than just addressing the connectors, hence drawing on the company’s vast experience in designing for harsh environments.

The final solution featured a combination of O-rings and proprietary methodology to protect the connector, and thus the PLB, from moisture ingress under seawater at depths down to 20m.

Notably, rigorous testing by Telliconnect and the PLB manufacturer proved that the new connector design was able to protect the equipment to an equivalent depth of 60m, exceeding the original product requirements and providing the customer with a healthy threefold safety factor.

The standard method employed to test connectors is pressurisation of the connectors using compressed air, followed by immersion in water and subsequently checking for air bubbles as a sign of leakage. This is simple enough to be used as an in process operation and can quickly and easily highlight any process or assembly problems.

In addition to the sealing requirements, the resultant connectors are designed to meet all the relevant Mil specs, durability requirements, electrical, mechanical, and environmental conditions that all standard military equipment needs to withstand to be able to operate in an airborne or seaborne environment.

And of course now, Telliconnect has incorporated this waterproofing process for TNC connectors into many of its other products including the N series, SMA, and custom designs such as the ABMS, an MCX derivative used for a cochlear implant, and the MPNC four way multi-pin connector for environmental corrosion monitoring.

These connector and adapter devices now form the company’s Pisces range and other applications include traffic monitoring systems, rail traction systems, military and aerospace applications, medical, marine radar, battery power, and corrosion monitoring for the oil and gas industry.

Telliconnect is a UK manufacturer of RF connectors and cable assemblies, based in Chelmsford and with facilities in the USA. It specialises in the design and manufacture of waterproof connectors, with the capability to design, develop and supply interconnect solutions to customer driven specifications in weeks not months.

More from Telliconnect

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True Grid Independence

Linear Technology’s George H Barbehenn outlines the company’s robust energy harvesting system for wireless sensors using a piezoelectric energy harvesting power supply and Li-Poly batteries with a shunt charger.

There’s an emerging and potentially large market for wireless sensors. By their very nature, wireless sensors are chosen for use in inaccessible places or for applications that require large numbers of sensors: too many to easily hardwire to a data network.

In most cases, it is impractical for these systems to run off primary batteries. For example, a sensor for monitoring the temperature of meat as it is shipped would need to be mounted in a tamper-proof way. Alternatively, HVAC sensors mounted on every source of conditioned air would be far too distributed to feasibly use batteries. In these applications, energy harvesting can solve the problem of providing power without primary batteries.

Energy harvesting alone often does not produce sufficient power to continuously run the sensor transmitter – energy harvesting can produce about 1~10mw, where the active sensor transmitter combination may need 100~250mw. Harvested energy must be stored when possible, ready for use by the sensor/transmitter, which must operate at a duty cycle that does not exceed the energy storage capabilities of the system. Likewise, the sensor/transmitter may need to operate at times when no energy is harvested.

Finally, if the stored energy is depleted and the system is going to shut down, the system may need to carry out housekeeping tasks first. This may include a shutdown message or storing information in non-volatile memory. Thus, it is important to continuously gauge available energy.

Complete energy harvesting system

Figure 1 shows a complete system implementation using an LTC3588-1 energy harvester and buck regulator IC, two LTC4071 shunt battery chargers, two GM Battery GMB301009 8mAh batteries and a simulated sensor transmitter modelled as a 12.4mA load with 1% duty cycle.
The LTC3588-1 contains a very low leakage bridge rectifier with inputs at PZ1 and PZ2 and outputs at $V_{in}$ and GND. $V_{in}$ is also the input power for a very low quiescent current buck regulator. The output voltage of the buck regulator is set by D1 and D0 to 3.3V.

The LTC3588 is driven by an Advanced Cerametrics PFCB-W14 piezoelectric transducer, capable of generating a maximum of 12mW. In our implementation, the PFCB-W14 provided about 2mW of power.

The LTC3588 is driven by an Advanced Cerametrics PFCB-W14 piezoelectric transducer, capable of generating a maximum of 12mW. In our implementation, the PFCB-W14 provided about 2mW of power.

The LTC4071 is a shunt battery charger with programmable float voltage and temperature compensation. The float voltage is set to 4.1V, with a tolerance on the float voltage of ±1%, yielding a maximum of 4.14V, safely below the maximum float allowed on the batteries. The LTC4071 also detects how hot the battery is via the NTC signal and reduces the float voltage at high temperature to maximise battery service life.

The LTC4071 is capable of shunting 50mA internally, says Microchip. However, when the battery is below the float voltage, the LTC4071 only draws ~600nA from the battery. The GM Battery GMB301009 batteries have a capacity of 8mAh and an internal series resistance of ~10Ω.

The simulated sensor transmitter is modelled on a Microchip PIC18LF14K22 and MRF24J40MA 2.4GHz IEEE standard 802.15.4 radio. The radio draws 23mA transmitting and 18mA receiving. The model represents this as a 12.4mA, 0.98% duty cycle (2ms/204ms) load, set with a self-clocked digital timer and a MOSFET switching a 267Ω resistor.

**Modes of operation**

This system has two modes of operation: charging sending and discharging sending. In charging sending mode, the batteries are charged while the sensor transmitter presents a 0.5% load. When discharging, the sensor

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**Figure 1:** Complete piezo based energy harvesting system independent of the grid. This design uses thin film batteries to gather energy collected by the piezo for a wireless sensor transmitter, which operates on a 1% duty cycle.
transmitter is operating but no energy is being harvested from the PFCB-W14.

**Charging sending**

When active, the PFCB-W14 delivers power at an average of around $9.2\,\text{V} \times 180\,\mu\text{A} \approx 1.7\,\text{mW}$. The available current must charge the battery and operate the buck regulator driving the simulated sensor transmitter. The active sensor transmitter draws $12.4\,\text{mA} \times 3.3\,\text{V} \approx 41\,\text{mW}$ at around 1% of the time, or about $0.41\,\text{mW}$ on average, leaving some current to charge the battery. Taking into account the 85% efficiency of the LTC3588 buck regulator, assuming an average $V_{\text{in}}$ of 9.2V, as shown in Figure 2, and a buck quiescent current of 8µA, the average current consumed by the system without charging the battery is:

$$I_{\text{AVG}} = \frac{I_{\text{SENSOR}} \bullet \text{DUTYCYCLE} + I_{\text{Q(BUCK)}}}{V_{\text{IN(AVG)}} \bullet \text{R(BUCK)}}$$

Harvested energy can drive the sensor transmitter at a 0.5% duty cycle with about 120µA left to charge the batteries. The GMB301009 batteries have a capacity of 8mAh, so they completely charge from empty in about 75 hours.

**Discharging sending**

When the PFCB-W14 is not delivering power, the voltage at $V_{\text{in}}$ drops to approximately:

$$I_{\text{AVG}} = \frac{12.4\,\text{mA}}{9.2\,\text{V}} \bullet 0.0098 + 8\,\mu\text{A} \approx 60\,\mu\text{A}$$

So the reflected load current calculation changes to:

$$\frac{8.4 + 6.6}{2} = 7.5\,\text{V}$$

The quiescent current of the buck regulator is higher because the regulator must switch more often to regulate from 7.5V versus 9.2V. At 78µA, with no energy harvested, the battery is discharged in around 115 hours. This indicates a charge storage capacity of >8.95mAh. These batteries when brand new could store approximately 12% more charge than rated.

A more serious problem is what happens when the battery is fully discharged. If current is drawn after the state of charge reaches zero, and the battery voltage drops below 2.1V, the battery is permanently damaged. Therefore the application must ensure that the battery voltage never falls below this limit. For this reason, battery cut-off is set to 2.7V or 3.2V to ensure some energy remains in the battery after the disconnect circuit has engaged.

Simply stopping the transmitter or disconnecting the load will not protect the battery, as the LTC4071 draws a quiescent current of approximately 600nA. Although this is extremely low, the total load, including the LTC3588V1, is nearly 2µA. A fully discharged battery will only be able to supply approximately 100µA before its voltage drops enough to damage the battery.

A disconnect circuit is necessary to ensure that the battery does not discharge in a reasonable amount of time. The LTC4071 provides an internal low battery disconnect circuit. This disconnect circuit was measured to provide <2nA of battery load at room temperature when activated. This leakage is typically dominated by PCB leakage. With only 2nA of battery drain current, the battery could survive for 50,000 hours in the discon-
nect state before the battery is damaged.

In Figure 3, the second battery (BAT2) is seen to disconnect 50 hours after BAT1 due to the 2µA load.

**Measured results**

The system shown in Figure 1 was measured in both operating modes: discharging-sending (Figure 3) and charging-sending (Figure 4).

**Discharging sending**

In Figure 3 the voltages of the two batteries BAT1, BAT2 and VBuck are plotted against time with the batteries supplying all the system energy, none from the PFCB-W14 piezo.

The batteries slowly discharge until BAT2 activates the LBO threshold of the LTC4071, whereupon the disconnect circuit activates and disconnects BAT2 from all circuitry except U5. This causes the voltage at Vin of the LTC3588 to drop below the UVLO for the regulator, and the regulator shuts off.

The load on BAT1 is the 2µA quiescent current of the LTC4071 and the LTC3588. This small load slowly discharges BAT1 until the low battery disconnect of LTC4071 is activated and BAT1 is disconnected.

**Charging sending**

When the PFCB-W14 once again starts delivering power to the system, Vin rises to 7V, which forward biases the body diodes of the LTC4071’s disconnect FETs. This charges the batteries until the reconnect threshold is reached, allowing batteries BAT1 and BAT2 to be reconnected. Looking at Figure 4, this can be seen as the voltage at Vin snaps down to the battery stack voltage.

Since the voltage at Vin is now VBAT1 + VBAT2 + (180µA×15k) = 6.2V, the buck regulator on the LTC3588 restarts and 3.3V is once again available.

**Conclusion**

With a few easy to use components, it is possible to build a complete compact energy harvesting power sub-system for wireless sensor transmitters. In this particular system a piezoelectric transducer supplies intermittent power, while two batteries store energy for use by the sensor transmitter. An integrated disconnect switch protects the batteries from over-discharge.

This system can fully charge the battery in 75 hours, even while operating the sensor transmitter at 0.5% duty cycle.

The batteries allow the system to continue operating the sensor transmitter at 0.5% duty cycle for 115 hours after the PFCB-W15 stops providing power. If longer battery operating time is required, the sensor transmitter duty cycle can be reduced to accommodate this need.

[More from Linear Technology](#)
Michael A. Briere discusses the first commercially viable application of GaN based power device technology, heralding a new era in power electronics through the combination of high performance and competitive costs for semiconductor power devices.

Since the advent of the spontaneous AlGaN-GaN based high electron mobility sheet formation, first discovered by M Asif Khan in 1991, significant effort has been made to bring the inherent capabilities of this exciting material system to bear in practical semiconductor power devices. The combination of high breakdown field strength due to the wide band gap of the III-nitrides, high electron mobility, as well as an unusually high channel electron density yield a remarkably compelling drift resistance.

Such devices also benefit from the reduced gate charge requirements involved in switching the devices on and off. Probably the most exciting attribute of the system involves the easily isolating nature of the inherently lateral devices, permitting unprecedented monolithic
integration of power systems. From a technologist’s point of view, it is unfortunate that, as in many such inherently superior technological alternatives, economics more than physics will determine the rate and extent of adoption of GaN based power devices.

The driving metric for adopting new semiconductor technologies is performance/cost. This is the same as used in the popular Moore’s Law for data processing technology. It is therefore imperative that focus be placed not on performance alone but at least equally on the fundamental factors that drive the economics of the technological proposition. In order to beat silicon, it is best to stay as close to the incumbent silicon platform as possible, only deviating when required.

In the case of GaN based power devices, one of the single greatest factors affecting cost is the choice of substrate material. As the adoption of any new device structure must compete with that of the incumbent, the cost of substrate and epitaxial growth should not far exceed the cost for a comparable fully fabricated silicon device.

This sets an upper limit of about $3/cm² for the combined cost of substrate and epitaxial layer. Only silicon substrates meet this requirement. The use of silicon substrates for GaN hetero-epitaxy present several significant technical challenges due to large mismatches in thermal co-efficient of expansion as well as lattice constants of the materials. As a technologist, such a challenge must be met and not avoided.

In addition, device fabrication processing costs must be competitive with CMOS based silicon processing often performed in large scale foundries processing >20,000 wafers/week. Therefore, in order to achieve the required performance/cost, GaN based devices should be processed in the same high volume foundries, using as much of the same high throughput, high yielding process technologies as used for silicon based devices as possible. Today, this requires that the substrates be at least 150mm, preferably 200mm.

Device performance requirements are not limited to such figures of merit as on-resistance or gate charge. Leakage currents, for instance, should achieve the performance levels of incumbent silicon devices. This is to say that the
criteria for both breakdown voltage and leakage currents (gate and source to drain) must be adjusted down from that commonly used when discussing GaN based devices of mA/mm of gate periphery to a more practical 0.1~1μA/mm. In addition, device quality, stability and reliability are all to be considered first order requirements for successful commercialisation of any new technology, with the incumbent silicon platform setting the standard.

A technological platform that meets the performance and cost requirements described above has been developed by International Rectifier, referred to as GaNpowIR. This platform uses multi-wafer MOCVD reactors to grow GaN epitaxy on standard 675μm thickness 150mm silicon substrates. Wafer bow for 2μm of epitaxial films is routinely less than 20μm. The device processing is fully compatible with silicon CMOS foundries and is based on thin film photo and etch lithography. The ohmic contacts are formed without the use of gold metallurgy.

Epitaxial quality is excellent, rivalling the published performance of any such film. Fabricated low voltage devices routinely exhibit Ion/Ioff ratios of >1012 with leakage currents less than 0.1μA/mm. In fact high voltage devices have been routinely shown to exhibit Ion/Ioff ratios in excess of 107, where Ioff is measured at 600V at less than 0.1μA/mm. In addition, the use of an insulated gate provides gate leakage currents of less than 0.1pA/mm as shown in Figure 1. In addition, excellent device ruggedness in the form of forward biased safe operating area, shown in Figure 2, and longterm stability of parametric performance such as Rdson as well as drain and gate leakage currents have been demonstrated to >6000hr. In fact, to date, over 3million device hours under accelerated stress conditions have demonstrated stable parametric behaviour for initial GaN based devices. See Figures 3 & 4.

More from International Rectifier

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Efficient Power Solutions For LED Lighting Installations

Cor van Dam, Avnet Abacus’s Marketing Director, reviews best practice in developing efficient power supply solutions for solid state lighting.

The LED lighting market looks set to explode, with some sources predicting that in five years time 50% of the global lighting market will be fulfilled by solid state solutions. Whether street or office illumination, refrigeration or architectural lighting, every solid state light needs power. And the power supply is often the weakest link.

Whilst the LEDs themselves are highly efficient, the benefits of this can be lost if energy efficiency is not optimised in the power supply. Correctly installed, the lifetime of an LED light can be 35 years or more but even a well designed power supply working within its operating parameters will last only 10~12 years. A poorly designed, lower efficiency power supply unit running at high temperature will not even last half as long.

Designing a power supply unit to achieve maximum operating efficiencies for LED lighting applications can be a daunting task. Designers have to consider a wide range of issues when conceiving power solutions to navigate the regulations for LED installations and ensure a power supply with maximum service life.

Regulations

Due to specific operating voltages and the configuration in which the LEDs are arranged, a standard power supply cannot be used with LED lighting. LED power supplies are governed by specific legislation: EN61347-1/-2-13, UL8750, UL1310 Class 2 for safety, EN55015 for EMC and EN61000-3-2 Class C for harmonics. But not all these specs are relevant to lighting applications.

In addition, the EU Ecodesign Directive 2009/125/EC sets out rules for reducing the
environmental impact of Energy using Products, EuP and other Energy related Products, ErP, at all stages from design concept to manufacturing. Street, office and domestic lighting all fall within this directive, along with their respective power supplies.

This legislation can sometimes be complicated to interpret for lighting designers and LED engineers entering the market, so discussing specific requirements with a specialist distributor such as Avnet Abacus with its comprehensive power portfolio and consultative approach can be valuable at the design stage to ensure compliance from the start.

In addition, a good distributor will work with its suppliers to keep up with future regulations and also participate in regular training.

Operating Efficiencies

The illumination output of solid state systems depends on how the LED array is driven. For example, using a constant current power supply produces the lowest cost and highest efficiency solution but unbalanced current for each parallel branch of LEDs can lead to uneven brightness and shortened life.

On the other hand, using a constant voltage power supply with an LED driver IC will accurately control the current through the LEDs, delivering a more uniform light output and long life, but at a reduced efficiency and a higher cost.

Designers will need to consider what application they are designing for and if a return on investment could be achieved by using a more expensive but more uniform driver solution to give extended life, instead of a low cost, reduced life option.

For small and medium power LED Lighting systems, for example, sophisticated semiconductor solutions from Power Integrations could be specified. PI leads on technology solutions to design customised LED power supplies with the minimum of component with their perfect working software tools.

This could be a low cost option for large volume applications, and one benefit, for example, is that the circuit can be trimmed for the highest efficiency.

However, this is not always the option with the fastest turnaround time, given the approval process required for some regulations.

The alternative is a ready to use, high quality, highly efficient off the shelf solution resulting in a faster time to market.

Typically the company has over 500 different models available with constant current output power of 3~350W, and a growing number with dimming options for use in applications such as architectural lighting. In addition, a wide range of LED power sup-
plies with constant voltage output are available, ranging from 10W to thousands of Watts, suitable for low to high power LED lighting systems and screens.

**Maximising service life**

Much has been written about the longevity of LEDs but it is important to be aware that they are not indestructible. A simple voltage glitch has the capacity to damage the LED. Aside from that, the main area affecting service life of both the power supply and LED lighting is that of excess heat.

Although the LED devices run at low power, the build-up of heat in the array as well as in the power supply needs to be minimised by using heat sinks on mountings for example. Not only will the lighting unit run more efficiently at a lower temperature but the risk of damage to the housing holding the LEDs will be significantly reduced.

Designers should be integrating heat dissipation solutions into the power supply design from the outset in order to maximise service life. Consideration should also be given to where and how the lighting units will be mounted to aid the cooling process.

Another issue to weigh up is minimising weak points within the power supply assembly itself. Components such as electrolytic capacitors and opto couplers are known to impact on service life and reliability. Increasingly, designers are specifying power supply solutions without these items.

In addition, care should be taken to ensure that high quality construction methods are used to prevent against the potential degradation caused by heat, aggressive moisture ingress and UV light. A dry solder joint from poor quality construction methods could prove critical once the power supply is in the field.

Selecting a power supply for LED lighting applications is not straightforward, and not everyone will have the in-depth knowledge of the rules and regulations that must be complied with in each specific market.

In order to achieve the longest life cycle possible with LED lighting, it is crucial to get the right advice and specify and select the correct power supply from the many solutions available and install it correctly. Only when all these things have been taken into consideration can you expect to achieve the most efficient solution possible.

More from Avnet Abacus

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AS one of Europe’s leading power, interconnect, passive, and electromechanical distributors, Avnet Abacus is teaming up with some of the world’s leading manufacturers of power components to deliver a series of free technical seminars in five locations across Europe focused on the difficult challenges that face power system design engineers.

In the one day sessions, the company, together with its franchises Aimtec, Cymbet, Emerson, Enpiron, Excelsys, Murata Power Solutions, Power Integrations and Schaffner are providing an overview of environmental and energy efficient directives impacting power supply design.

Explains Cor van Dam, Avnet Abacus’s European Marketing Director, “Efficient use of power is a challenge that affects everyone. There are many issues: new mandatory regulations will require stand-by (no-load) energy consumption to approach zero watts; consumer demands that battery powered devices have a long life between recharging; and LED lighting systems must be powered correctly or the benefits are wasted. Our seminar series will address these topics and many more, and we encourage design engineers to raise their own specific areas of interest during the extensive Q&A sessions with technical representatives from the participating companies.”

The event will also feature tabletop presentations from leading manufacturers of associated power products including Molex, Pulse and TE Connectivity.

The seminars are scheduled for October 4 at the Novotel Charenton, Paris, October 12 at Avnet Abacus’s Milan office, October 20 at the company’s Stuttgart office, October 25 at Avnet Abacus Munich and November 3 at the Newbury UK office of Avnet Abacus.

You can sign up for the free seminars at http://www.avnet-abacus.eu/power or telephone +44 (0) 1628 512 940.
The world of defence procurement has not escaped financial clampdown and deep cuts. Whilst attempts have been made to offset the reduction in man power via an increased use of technology, the cost of electronic systems is also now under the spotlight of severe scrutiny.

The days when ‘defence budget’ could be read as ‘unlimited budget’ are long gone – if indeed that misconception was ever true and not based mostly on newspaper myth. What is certainly now true, however, is that defence spending is under the microscope.

Armed forces worldwide are being forced to implement cost-reduction plans yet the basic demands made of the equipment they use has not changed: it must operate reliably for extended periods under the harshest of conditions, withstanding extremes of shock, vibration and temperature, often in the open air where it is exposed to rain and humidity, the ingress of dust and sand and potentially other gases and pollutants.

Electronics systems are especially vulnerable to the hazards described above. Equally, makers of equipment used for military and aerospace applications are under increasing competitive price pressure. In many circumstances the answer may lie in implementing smarter design practices, enabling the use of components which may not carry a full military release – nor a full military price tag.

Here are some pointers that may help:

- Avoid DSCC drawings if at all possible. Instead choose QPL or EPPL parts.
- Try to remove high palladium content parts such as ceramic capacitors manufactured using ‘wet processes’ from designs. The price of palladium continues to rise and with supply still limited these parts are likely to increase in price throughout the year.
- Tantalum, like palladium, is still in short supply. Throughout 2010 the tantalum industry’s consumption of material exceeded production and projections indicate that there will be continued shortages for six to nine months. To this end tantalum prices are predicted to raise well into 1H 2011.

Wet tantalum capacitors are especially expensive and often on an extended lead time, however some suppliers like AVX have secured powder and wire supplies for 3~5 years and anticipate no impact on any of their Hi-Rel tantalum parts. Wet tantalums offer higher CV,
long operating life and meet the vibration and shock requirements of military applications.

However there are new technologies now available such as Kemet’s polymer hermetic seal devices which reduce the number of components required on the board, offer lighter weight and have low and stable ESR across temperature and frequency range.

Can plastic bodied connectors be used instead of metal shells? Plastics and composites technologies have moved on a great deal, and not only are non-metal shelled connectors cheaper, they are also lighter.

The COTS approach

Then of course there is the COTS Commercial Off the Shelf approach. John McHale of USA magazine Military & Aerospace Electronics has an interesting take. “Basically everyone has a different definition of COTS from the military programme manager all the way down to the component vendor,” he says.

Maybe it is as one defence supplier says, COTS is whatever my customer says it is.

Cynicism aside, some manufacturers such as AVX have available AEC-Q200 Commercial Off the Shelf Plus parts, that is COTS devices, with up-screening to increase the level of testing. Passive component manufacturers such as AVX, Kemet, Syfer and Vishay now provide a wide variety of testing options giving you the flexibility to pick the testing required to meet your actual design requirements.

Issues to consider

Although COTS parts may provide a viable option, there are possible issues to consider. COTS components will usually have a shorter lifecycle and while full Mil Spec devices are rated over the full temperature range, commercial parts may only be rated over a much narrower range.

COTS devices are unlikely to have the same traceability as full Mil Spec components. Also, the design and manufacturing processing techniques and even locations of COTS products are changed frequently which may impact on their usefulness for military applications.

But perhaps the most difficult issue to consider when assessing the value of COTS components is obsolescence.

Previously, military systems designers relied heavily on a procurement system that had a policy of maintaining longterm spare parts availability with detailed records. Therefore, engineers could easily assess the reliability and quality of available spare parts, and as a consequence did not have to concern themselves with obsolescence management.

However, with COTS parts, the situation is different and manufacturers may cease manufacture of specific parts with only six months to one year’s warning. Finally, COTS parts are more likely to suffer from the problem of counterfeiting, since the traceability is not so rigorous.

TTI sports a Europe-wide focus team supporting military, aerospace and space customers. Part of the company’s brief is to help suggest ways in which design engineers can reduce cost and ensure component supply. The company regularly works with engineering teams to create preferred parts lists, taking advantage of design-in synergy across multiple sites to reduce inventory held by the customer, increase quantity and reduce costs.

Above all, hi-rel customers – even more so than for other applications – must only procure from authorised distributors. This reduces incoming inspection and the risk of using counterfeit products, and should result in cost savings without compromising system reliability!

You can see TTI at the DSEi show at London’s ExCeL, September 13–16.
Until a few years ago really complex and high speed designs were required only for extremely high tech and high volume products such as PC motherboards and were designed using expensive CAD packages.

As these technologies are slowly appearing in more common products, more PCB designers have to do tightly controlled, high speed PCB designs. Whilst it is easy to justify $30k+/license CAD for mass produced products, this price tag is a barrier for smaller companies trying to implement new designs. They simply can’t afford professional, expensive CAD and have to find their way in implementing the new technologies with cheaper software such as Altium Designer.

Cheaper software packages do not have quite the same level of high speed design features as expensive CAD but by using some workarounds it is possible to meet the challenge.

In this article I explain how to use Altium Designer 10 for designs that were traditionally done using more expensive CAD. There are however minimum requirements, for example real time measuring the track lengths, and for very advanced designs such as 64bit memory down, we have to measure pad to pad lengths on multipoint nets as well. It is also required to be able to place meander structures automatically and to do differential pair routing. Altium Designer meets these minimum requirements, although there are some important features missing, for example package length support and some bugs need fixing related to DRC in ‘diffpair to diffpair’ or ‘net segment length matching’.

Connection objects

In Altium, just like in other PCB design software, we create design objects and then constraints referring to those objects. Some get created during schematics design, while others have to be created in the PCB editor. They define the connections in a circuit, a group of connections or the way of making the connections such as differential pair routing.

Differential pairs

For differential signals, we create differential pair objects. We give Net names for both the positive and the negative net with ‚P’ and ‚N’ suffixes, add Net Class directives and a Diffpair directive on both wires in the schematics drawing.

![Figure 1: Net name, Differential Pair and Net Class specification in schematics](image)

From-Tos

The „From-To” objects define pin to pin connections on multipoint nets. With these objects, we can control the propagation delay from one pin to another. To create the From-Tos, use the PCB Panel’s „From-To Editor” in the top drop down list. Unfortunately, with the current version of Altium Designer we have to create these
Figure 2: Jede specification for DDR3 memory module with Altium From-To objects

on every net, manually, one by one, unlike in Cadence Allegro by applying a SigXplorer-created ECSet on a group of nets. Typical examples where From-Tos are required are the different DIMM memory card designs, memory down configurations, multiple-DIMM/channel motherboard designs, Compact-PCI systems and so on.

Classes

Classes are also design objects: they are groups of other design objects, for example Net, Differential Pair, From-To or Component Classes. We can manually create classes in the PCB Editor’s „Object Class Explorer” window and (only net classes) in the schematics graphically.

Design rules or constraints

In Altium Designer we usually specify PCB design rules or constraints in the Design Rules editor, although we can specify some of them in the schematics level as well, by graphically attaching the PCB Layout directive symbol to net or to (copies) multiple nets. Some design rules control interactive PCB editing parameters, others are checked by an on-line Design Rule Check (DRC), while yet other rules are checked by the manually run DRC.

The trace width and spacing rules are based on manufacturing capabilities and impedance calculations. The length rule values come from static timing analysis or signal integrity analysis; other times they are standardised and described in a standard such as Jede JESD21C DDR-memory DIMM design documents or PICMG documents, or in a processor’s motherboard design guide.

Rule checking on From-Tos and diffpairs in general doesn’t work well in Altium Designer 10. Often the DRC does not report a violation when there is one, so for their control we have to manually check/calculate lengths on the PCB Panel. Sometimes the DRC and the On-Line DRC ignore some matching rules, especially on diffpairs or From-Tos, or it ignores a few of the objects in the rule.

Because of this, we have to validate every length related rule by running a trace and checking if a new violation shows up after running DRC. If not, then we have to re-create the rule with a new name and delete the original one.

Trace Width

Normally we put a group of nets based on characteristic impedance into a Net Class. Then we set up a „Width” rule for every net class separately.
Spacing

Spacing in PCB design has two aspects: manufacturability and controlling crosstalk. For the first aspect, we set up a „Clearance” rule and for the second type, we use the „Parallel Segment” rule which ignores short segments, since those are not significant in the aspect of crosstalk.

Differential pair rule

The „Differential Pair Routing” rule has to be set up for every Differential Pair Class. The rule specifies the trace spacing between the positive and negative traces of the differential pair.

<table>
<thead>
<tr>
<th>Case</th>
<th>Objects to create</th>
<th>Design Rules (on objects)</th>
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</thead>
<tbody>
<tr>
<td>Trace Width</td>
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<td></td>
</tr>
<tr>
<td>Spacing</td>
<td>• Net Class or DP Class</td>
<td>• Clearance rule (on Net Class(es))</td>
</tr>
<tr>
<td></td>
<td>• Net Class or DP Class</td>
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<tr>
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<td>• Diffpair</td>
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<tr>
<td></td>
<td>• DP Class</td>
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<tr>
<td></td>
<td>• Net Class</td>
<td>• Matched Net Lengths rule (Phase tolerance, on DP Class. „Within Differential Pair”=On, others=Off)</td>
</tr>
<tr>
<td>Min/Max Trace Length</td>
<td>• Net/DP/From-To list or Class</td>
<td>• Matched Net Lengths rule (on Net Class)</td>
</tr>
<tr>
<td>Match nets on Point to point bus</td>
<td>• Net Class</td>
<td>• Width rule (on Net Class)</td>
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<tr>
<td></td>
<td>• Differential Pair Classes, one for each matching group</td>
<td></td>
</tr>
<tr>
<td>Match diffpairs on a multi-lane Point to point bus</td>
<td>• Diffpair</td>
<td>• Diffpair rule (on DP Class)</td>
</tr>
<tr>
<td></td>
<td>• Net Class</td>
<td>• Width rule (on Net Class)</td>
</tr>
<tr>
<td></td>
<td>• Differential Pair Classes, one for each matching group</td>
<td>• Matched Net Lengths rule (Phase tolerance, on DP Class. „Within Differential Pair”=On, others=Off)</td>
</tr>
<tr>
<td>Match Net Segment Lengths</td>
<td>• From-Tos: every controlled segment on every net.</td>
<td>• Matched Net Lengths rule (on From-To Class). One separate rule for each controlled segment.</td>
</tr>
<tr>
<td></td>
<td>• From-To Class: Same segment on different nets. Every controlled segment is a separate From-To Class.</td>
<td>• Length Rule (on all segment’s From-Tos together).</td>
</tr>
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<td></td>
<td>• From-Tos: every controlled segment on every net.</td>
<td>• Matched Net Lengths rule (Phase tolerance, on From-To Class. „Within Differential Pair”=On, others=Off). One separate rule for each controlled segment.</td>
</tr>
<tr>
<td></td>
<td>• From-To Class: Same segment on different nets.</td>
<td>• Matched Net Lengths rule (Group Match, on From-To Class. „Within Differential Pair”=Off, others=On). One separate rule for each controlled segment.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Length Rule (min/max) on all segment’s From-Tos together.</td>
</tr>
<tr>
<td>Match Net Segments on balanced Tree topology</td>
<td>• From-Tos: From-Tos are defined in the Master device to each Slave direction.</td>
<td>• Matched Net Lengths rule (on the one and only From-To-Class).</td>
</tr>
<tr>
<td></td>
<td>• From-To Class: All nets in group from the master to every slave device.</td>
<td>• Length Rule (on all segment’s From-Tos together).</td>
</tr>
</tbody>
</table>

Table 1: Objects and rules
and negative track within the pair, and it is enforced in interactive editing when we use the Interactive Differential Pair routing option. For every DP class we need two more rules – „Width” and „Matched Net Lengths” – to meet the phase tolerance requirements.

**Net Length Rule**

With this rule, we can specify a minimum and maximum trace length for a group of signals such as Net Class or Differential Pair Class, or a group of From-Tos.

**Matched Net Length Rule**

With this rule we can control the trace lengths relative to each other in a group of signals, diff-pairs or From-Tos. A parameter of the rule specifies the types of objects to be applied on: „Within Differential Pair” (for DP phase tolerance), „Between Differential Pairs” (DP to DP matching, like DVI, Hyper Transport), „Between Nets” (for net-matching). See Table 1.

**Interactive editing**

During interactive editing or routing we have to measure the trace lengths in real time for length meter or gauge, or quasi real time for PCB Panel.

The Gauge pops up during „Interactive Length tuning” or during „Interactive Differential Pair Length tuning” which shows total net lengths in real time. The tuning parameters can be set up during tuning when we hit the TAB key.

Unfortunately, this only works on total net length, not on segment From-To lengths, and it does not pop up during routing or during sliding/stretching of trace segments, like it would in Cadence Allegro.

The PCB Panel shows lengths in quasi real time, which means that first we tune/slide/route, then press ESCAPE, then the values get updated. We can see the length of the other traces in a class in the list. The PCB Panel has differ-
ent Tabs for different object types, such as Nets, Diffpairs or From-Tos.

The Rules&Violations panel lists all the rules and related violations with violation details such as deviation from preferred length. Some are quasi real-time, others require to rerun the DRC.

Figure 3: On-screen Length Meter during „Tuning“

We select the Net Class on the PCB Panel’s Nets tab and then sort the member nets by length, then shorten the longest ones, calculate a minimum length which is the longest–delta, then lengthen the shorter ones until the Length meter becomes green for every signal.

Diffpair phase tolerance matching
The differential pairs need to be balanced, so the length of the negative net relative to the positive net of the same pair has to be matched. If the pair is unbalanced, then we get signal integrity problems, such as eye closure, increased common mode noise due to „mode transformation“, increased crosstalk and increased EMI. The phase tolerance requirement is specified in processor datasheets, design guides or standards. For example for PCI-Express 1.1 we usually use +/-0.125mm.

Diffpair to diffpair matching
There is a need for diffpair to diffpair matching in multi-lane, high speed serial interfaces such as PCI-Express, DVI or Hyper-Transport. The design of these interfaces has to be done similarly to the net matching but with the rule parameters set to only „Check Nets Within Differential Pair“, and we use the Diffpairs Editor tab instead of the Nets tab.

Net segment length control
Altium has minimal support for net segment length control. It is possible to implement designs with it but it needs lots of workarounds and manual calculations. Unfortunately, the DRC ignores rules on From-Tos, so we have to check manually during editing. We check the From-To lengths on the PCB Panel’s From-To Editor, and the total net length, comparing with our calculations, on the gauge. First we hand route the tracks to follow the specified topology, then we tune the appropriate track segments.

Matching From-To lengths is different from net to net matching, since we cannot see a list of all From-Tos on the same segment of different nets in a single list: we have to browse the nets first.
When using the on-screen length meter, we can see only the total net length that has to be within a manually calculated range separately for each From-To of each net.

In Cadence Allegro, for example, these two problems don’t exist while working with the Constraint Manager, so for Altium Designer users, segment matching is a manual job and more time consuming. The required manual calculation is the new total length for each segment on each net to be used in the on-screen length meter.

\[
\text{New\_Total\_Length} = \text{actual\_total\_length} + (\text{required\_segment\_length} - \text{actual\_segment\_length})
\]

The From-To Editor sometimes displays an incorrect length for the From-Tos. The cause is that Altium Designer is unable to measure partial track segment lengths. To avoid this, we should route the tracks in a way that they break at every branch. If this still doesn’t fix it, then we have to delete and then re-route those segments.

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**Package length**

Unfortunately, there isn’t any support for this in Altium Designer. For large FC-BGA packages the signal routing lengths inside the package are usually non-matched, each signal is routed at a different random length. The information is usually provided in an Excel spreadsheet as a Trace Length Calculator or in a design guide or datasheet.

The point in length control is to ensure proper timing at chip receiver circuits and not at the package balls. The design software should measure/control the total lengths made of package and PCB lengths summed together.

Other programs such as Cadence Allegro have this feature built-in as „Pin Delay“ for library components. The only possible workaround is to manually set up absolute length rules individually for each net, which can be 100~200 rules on some interfaces, and possibly create new Excel calculators for each design.

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**Figure 6: Package Length**

**Wish list**

For really complex and high speed designs, a few important features should be implemented in Altium Designer:

- Package length support for large BGA devices.
- Importing design rules from Excel spreadsheet.
- Automatically generate From-Tos for all nets in a group or Class, based on user defined graphical topology. In Cadence Allegro we create pin-pairs on one net, then create a rule that contains the topology relative to component designators, then apply the rule for all nets in a group.
- Length Meter improvements needed: Display From-To lengths as well. Pop up during routing and sliding as well, display one gauge per rule.
- Colour coding of length parameters on the PCB panel based on DRC pass/fail.
- When we select a From-To on the From-To Editor, it should highlight the related track segments, and editing should not be disabled.

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